signetics

mos fets

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D-MOS FET - SINGLE GATE N-CHANNEL ENHANCEMENT

UHF AND GENERAL PURPOSE RF APPLICATIONS

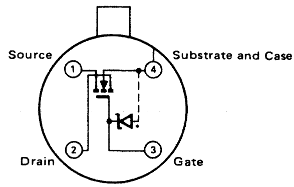
SD200 SD201 SD202 SD203

DESCRIPTION

The Signetics D-MOS SD200/201/202/203 are silicon, insulated gate, field effect transistors of the N-channel enhancement mode type. They are fabricated by the Signetics double-diffused process which gives superior high frequency performance up to 2GHz. A zener diode is connected between the gate and substrate of the SD201 and 203 that bypasses any voltage transient lying outside the range of −0.3V to +25.0V. Thus the gates of the SD201 and 203 are protected against damage in all normal handling and operating situations.

All four devices are general purpose transistors especially suited for amplifier designs in the UHF range (500MHz to 2GHz). They have extremely high transconductance, very low input capacitance and extremely low feedback capacitance. The SD200, 201, 202 and 203 combine high gain with low levels of noise, intermodulation distortion and feedback capacitance. These parameters make them ideally suited for critical amplifier applications. These devices are hermetically sealed in modified 4-lead TO-72 packages.

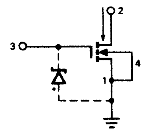
PIN CONFIGURATION (Top View)



Order Part Nos: SD200DC, SD201DC, SD202DC, SD203DC

*Diode Protection On SD201, SD203 Only.

COMMON SOURCE BIAS SCHEME



$+V_{DS}$ = 0 → +20 Volts
$+V_{GS}$ = 0 → +4 Volts
$+I_{DS}$ = 0 → +20mA

*Diode Protection On SD201, SD203 Only.

GENERAL FEATURES

- ION-IMPLANTED FOR GREATER CONTROL AND RELIABILITY
- WIDE DYNAMIC RANGE
- POSITIVE BIAS ONLY

SD200/201 FEATURES

- HIGH GAIN THROUGH UHF RANGE – 10dB AT 1GHz
- LOW NOISE THROUGH UHF RANGE:
  SD200 – 4.5dB
  SD201 – 5.0dB
- LOW INPUT CAPACITANCE – 2.4pF
- LOW FEEDBACK CAPACITANCE – 0.20pF
- HIGH DRAIN-TO-SOURCE VOLTAGE – +30V
- HIGH FORWARD TRANSCONDUCTANCE – 15,000 μmhos

SD202/203 FEATURES

- HIGH GAIN THROUGH UHF RANGE – 10dB AT 1.5GHz
- LOW NOISE THROUGH UHF RANGE – 3.2dB AT 1.0GHz
- LOW INPUT CAPACITANCE – 3.0pF
- LOW FEEDBACK CAPACITANCE – 0.20pF
- HIGH DRAIN-TO-SOURCE VOLTAGE – +25V
- HIGH FORWARD TRANSCONDUCTANCE – 20,000 μmhos

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C (Unless Otherwise Noted)

Drain-To-Source Voltage (V_{DS})	
SD200/SD201	+25V
SD202/SD203	+20V
Drain-To-Substrate Voltage (V_{DB})	
SD200/SD201	+25V
SD202/SD203	+20V
DC Gate-To-Substrate Voltage (V_{GB})	
SD200	±40V
SD201	−0.3V, +10V
SD202	±40V
SD203	−0.3V, +10V
Drain Current (I_D)	50mA
Ambient Temperature Range	
Storage	−65°C to +175°C
Operating	−65°C to +125°C
Transistor Dissipation (P_T)	
At +25°C Case Temperature	1.2W
(Derate linearly to +125°C case temperature at the rate of 8.0mW/°C.)	
At +25°C Free-Air Temperature	300mW
(Derate linearly to +125°C free-air temperature at the rate of 2.0mW/°C.)	

ELECTRICAL CHARACTERISTICS

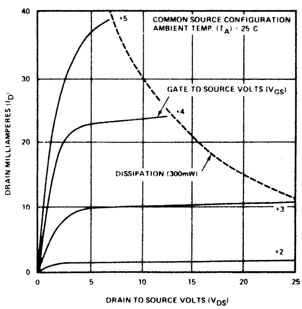
T_A = 25°C
(Unless Otherwise Noted)

PARAMETER	
BV_{DS}	Drain-To-Source Breakdown Voltage
I_{GSS}	Gate Leakage Current
I_D (OFF)	Drain-To-Source Current
I_{DSS}	Zero Bias Drain Current
V_T	Threshold Voltage
gfs	Forward Transconductance
Small Signal Short Circuit	
C_{ISS}	Input
C_{OSS}	Output
C_{RSS}	Reverse Transfer
Gps	Power Gain*
NF	Noise Figure*
r_{DS} (ON)	Drain-To-Source On Resistance
P_I	Intercept Point

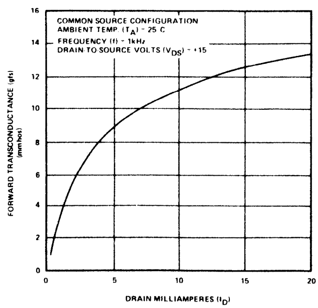
*Measured In Amplifier Test Fixture.

CHARACTERISTIC CURVES – SD200/201

DRAIN CURRENT VS DRAIN-TO-SOURCE VOLTAGE



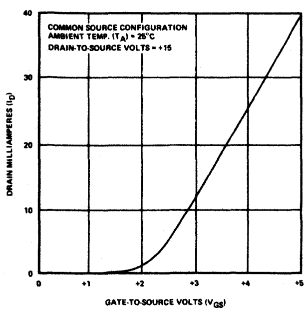
1kHz FORWARD TRANSCONDUCTANCE VS DRAIN CURRENT



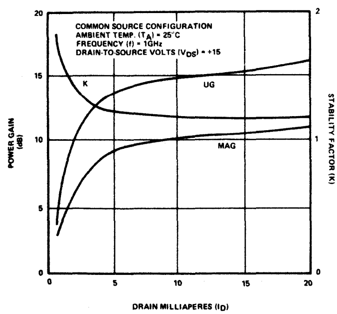
TEST CONDITIONS	SD200			SD201			SD202			SD203			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{GS} = 0V, I_D < 1μA	25	30		25	30		20	25		20	25		V
V_{GS} = ±10V, V_{DS} = 0V			0.1						0.1				nA
V_{GS} = +10V, V_{DS} = 0V					0.001	1.0					0.001	1.0	μA
V_{DS} = +15V, V_{GS} = 0V		0.001	1.0		0.001	1.0		0.001	1.0		0.001	1.0	μA
V_{DS} = +15V, V_{GS} = 0V		0.001	1.0		0.001	1.0		0.001	1.0		0.001	1.0	μA
V_{DS} = V_{GS} = V_T, I_D = 1μA	0.1	1.0	2.0	0.1	1.0	2.0	0.1	1.0	2.0	0.1	1.0	2.0	V
V_{DS} = +15V, I_D = 20mA, f = 1kHz													
V_{GS} ≅ +4V	13.0	15.0		13.0	15.0								mmhos
V_{GS} ≅ +2.5V							17.0	20.0		17.0	20.0		mmhos
V_{DS} = +15V, f = 1MHz													
I_D = 20mA		2.4	3.0		2.4	3.0		3.0	3.6		3.0	3.6	pF
I_D = 0A		1.0	1.2		1.0	1.2		1.0	1.2		1.0	1.2	pF
I_D = 0A		0.20	0.30		0.20	0.30		0.20	0.30		0.20	0.30	pF
V_{DS} = +15V, I_D = 20mA, f = 1GHz													
V_{GS} ≅ +4V	8	10		8	10								dB
V_{GS} ≅ +2.5V							8	10		8	10		dB
V_{GS} ≅ +4V		4.5	6.0		5.0	6.5							dB
V_{GS} ≅ +2.5V								3.5	4.5		4.0	5.0	
V_{GS} = +5V, I_D = 5mA		50	70		50	70		35	50		35	50	Ω
V_{DS} = 15V, I_D = 20mA, f = 1GHz, Δf = 2MHz		29			29			29			29		dBM

CHARACTERISTIC CURVES – SD200/201 (Continued)

DRAIN CURRENT VS GATE-TO-SOURCE VOLTAGE

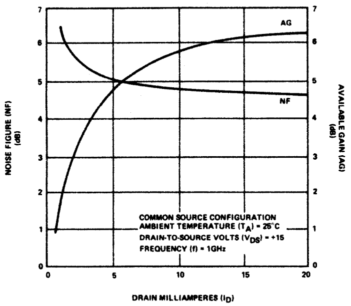


POWER GAIN VS DRAIN CURRENT

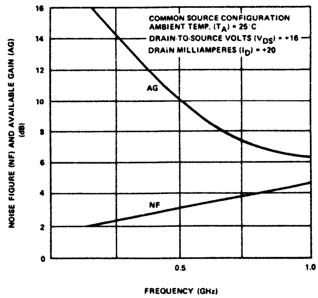


CHARACTERISTIC CURVES – SD200/201 (Continued)

NOISE FIGURE AND AVAILABLE GAIN VS DRAIN CURRENT



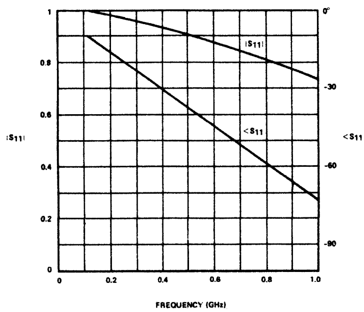
OPTIMUM NOISE FIGURE AND AVAILABLE GAIN VS FREQUENCY



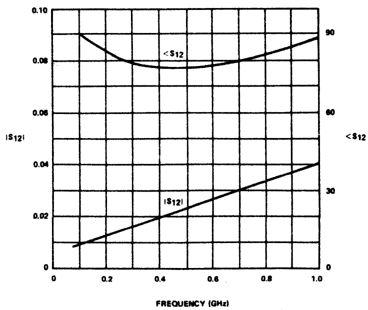
"S" PARAMETERS

COMMON SOURCE CONFIGURATION
AMBIENT TEMPERATURE (T_A) = 25°C
DRAIN MILLIAMPERES (I_D) = 20
DRAIN-TO-SOURCE VOLTS (V_{DS}) = +15

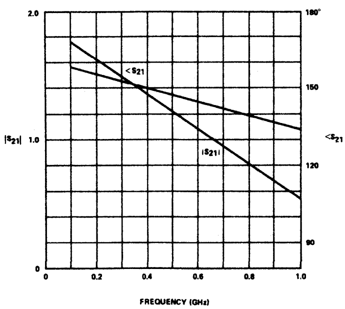
S_{11}



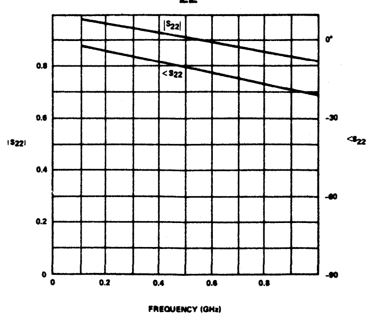
S_{12}



S_{21}

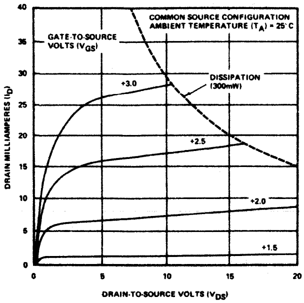


S_{22}

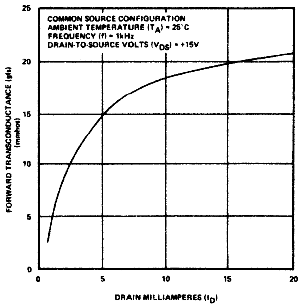


CHARACTERISTIC CURVES – SD202/203

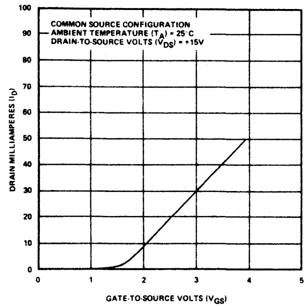
DRAIN CURRENT VS DRAIN-TO-SOURCE VOLTAGE



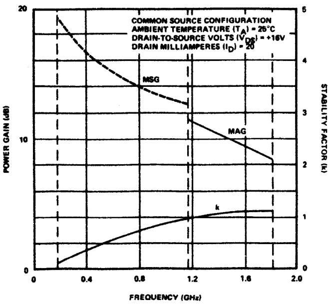
1kHz FORWARD TRANSCONDUCTANCE VS DRAIN CURRENT



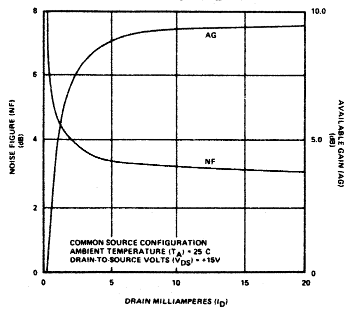
DRAIN CURRENT VS GATE-TO-SOURCE VOLTAGE



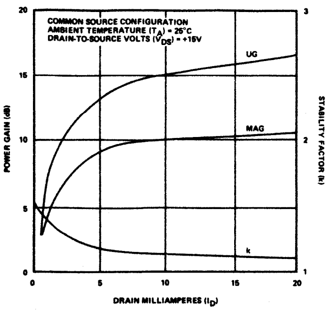
POWER GAIN VS FREQUENCY



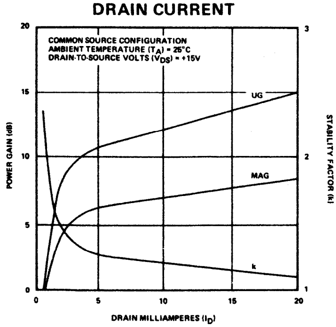
1.0GHz NOISE FIGURE AND AVAILABLE GAIN VS DRAIN CURRENT



1.5GHz POWER GAIN VS DRAIN CURRENT



1.8GHz POWER GAIN VS DRAIN CURRENT

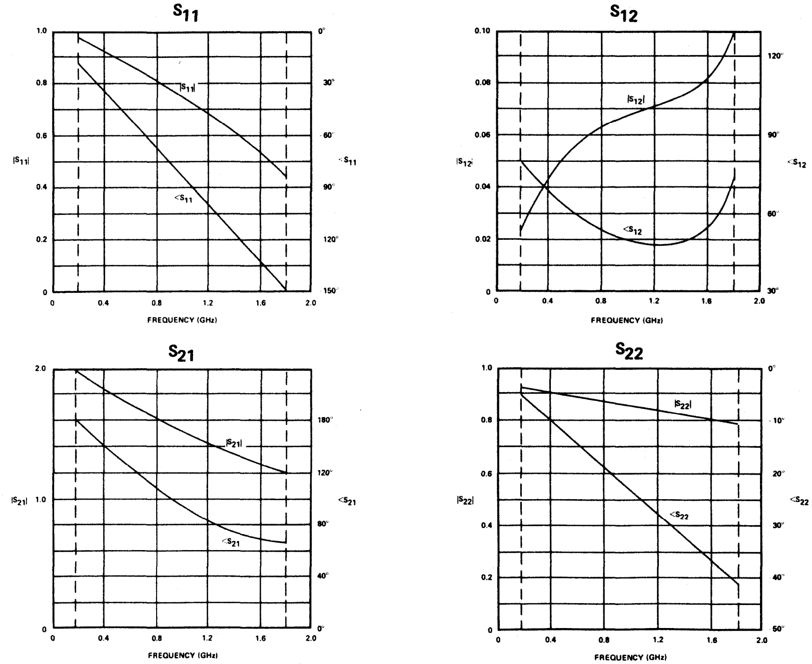


CHARACTERISTIC CURVES – SD202/203 (Continued)

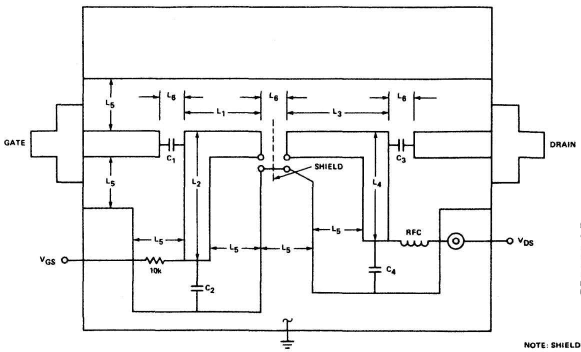
"S" PARAMETERS

COMMON SOURCE CONFIGURATION
AMBIENT TEMPERATURE (T_A) = 25°C

DRAIN MILLIAMPERES (I_D) = 20
DRAIN-TO-SOURCE VOLTS (V_{DS}) = +15



1GHz NOISE FIGURE AND POWER GAIN TEST FIXTURE



DIALECTRIC IS 1/16" TEFLON-FIBERGLASS (3M-K6096-11)
ALL MICROSTRIP WIDTH = 0.175"

L_1 = 0.48"
L_2 = 1.52"
L_3 = 0.64"
L_4 = 1.36"
L_5 = 5/16"
L_6 = 1/8"

$C_1 = C_2 = C_3$ = 0.8-10pF
Johanson 5201
C_4 = 1.20pF
Johanson 5501
RFC = 10 TURNS 26 AWG 1/4" DIA.
1000pF BYPASS
CORY FT4-01-2
LAUNCHERS – OSM248-2

NOTE: SHIELD AND 4 TUNABLE CAPACITORS ON GROUND PLANE SIDE OF AMPLIFIER.

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D-MOS FET SWITCH N-CHANNEL ENHANCEMENT

ANALOG AND DIGITAL SWITCH AND SWITCH DRIVER APPLICATIONS

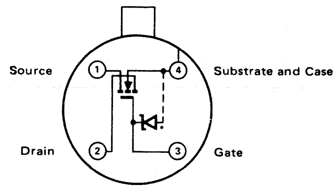
SD210 SD211 SD212 SD213 SD214 SD215

DESCRIPTION

The Signetics D-MOS SD210, 211, 212, 213, 214 and 215 are silicon, insulated gate, field effect transistors of the N-channel enhancement mode type. They are fabricated by the Signetics double-diffused process which gives high switching speed and low capacitance. A zener diode is connected between the gate and substrate of the SD211, 213 and 215. The diode bypasses any voltage transients which lie outside the range of −0.3V to +25V. Thus, the gate is protected against damage in all normal handling and operating situations. A drain-to-source breakdown of typically 35V makes the SD210 and 211 ideally suited for ±10V switch driver applications. Other characteristics allow them to be used as ±5V switches. The SD214 and 215 are designed to switch signals up to ±10V and the SD212 and 213 are designed to switch signals up to ±5V.

All the devices feature low gate node capacitance, extremely low drain node capacitance and very low feedback capacitance. Low "ON" resistance and hermetically sealed 4-lead TO-72 packages are also featured.

PIN CONFIGURATION (Top View)



*Diode protection on SD211/213/215 only.

Order Part Nos.
SD210DE, SD211DE, SD212DE,
SD213DE, SD214DE, SD215DE

FEATURES

- LOW FEEDBACK CAPACITANCE – 0.30pF
- LOW DRAIN NODE CAPACITANCE – 1.3pF
- LOW GATE NODE CAPACITANCE – 2.4pF
- LOW FEEDTHROUGH AND FEEDBACK TRANSIENTS
- ION-IMPLANTED FOR GREATER RELIABILITY
- EXCELLENT ISOLATION FROM INPUT TO OUTPUT – 120dB
- 35V DRAIN-TO-SOURCE VOLTAGE FOR SD210/211

APPLICATIONS

SWITCH DRIVER
ANALOG SWITCH
MULTIPLEXERS
DIGITAL SWITCH
SAMPLE AND HOLD
CHOPPERS
A-TO-D CONVERTERS
D-TO-A CONVERTERS

ABSOLUTE MAXIMUM RATINGS T_A = 25°C (Unless Otherwise Noted)

PARAMETER		SD210	SD211	SD212	SD213	SD214	SD215	UNITS
V_{DS}	Drain-to-Source	+30	+30	+10	+10	+20	+20	Vdc
V_{SD}	Source-to-Drain	+10	+10	+10	+10	+20	+20	Vdc
V_{DB}	Drain-to-Substrate	+15	+15	+15	+15	+25	+25	Vdc
V_{SB}	Source-to-Substrate	+15	+15	+15	+15	+25	+25	Vdc
V_{GS}	Gate-to-Source	±40	−15 +25	±40	−15 +25	±40	−25 +30	Vdc
V_{GB}	Gate-to-Substrate	±40	−0.3 +25	±40	−0.3 +25	±40	−0.3 +30	Vdc
V_{GD}	Gate-to-Drain	±40	−15 +25	±40	−15 +25	±40	−25 +30	Vdc

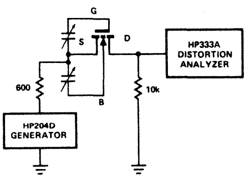
ABSOLUTE MAXIMUM RATINGS (All devices)

Drain Current (I_D) 50mA

Ambient Temperature Range
- Storage −65°C to +175°C
- Operating −65°C to +125°C

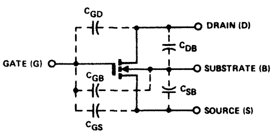
Transistor Dissipation (P_T)
- At 25°C Case Temperature 1.2W
  (Derate linearly to +125°C case temperature at the rate of 8.0mW/°C.)
- At 25°C Free-Air Temperature 300mW
  (Derate linearly to +125°C free-air temperature at the rate of 2.0mW/°C.)

DISTORTION TEST CIRCUIT



NOTE: ALL RESISTORS STANDARD AND ARE MEASURED IN OHMS.

CAPACITANCE MODEL



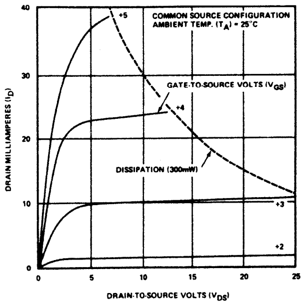
ELECTRICAL CHARACTERISTICS

PARAMETER	
Breakdown Voltage	
BV_{DS}	Drain-To-Source
BV_{SD}	Source-To-Drain
BV_{DB}	Drain-To-Substrate
BV_{SB}	Source-To-Substrate
Leakage Current	
I_{DS} (OFF)	Drain-To-Source
I_{SD} (OFF)	Source-To-Drain
I_{GB}	Gate
V_T	Threshold Voltage
gfs	Forward Transconductance
Small Signal Capacitances (See Capacitance Model)	
$C_{(GS+GD+GB)}$	Gate Node
$C_{(GD+DB)}$	Drain Node
$C_{(GS+SB)}$	Source Node
C_{DG}	Reverse Transfer
r_{DS} (ON)	Drain-To-Source Resistance

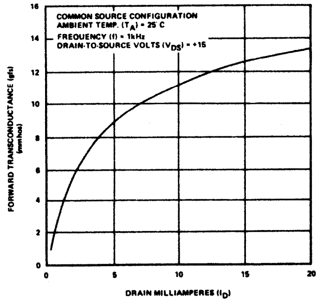
TEST CONDITIONS	SD210			SD211			SD212			SD213			SD214			SD215			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{GS} = V_{BS}$ = 0V, I_S = 10µA	30	35		30	35														V
$V_{GS} = V_{BS}$ = −5V, I_S = 10nA	10	25		10	25		10	25		10	25		20	25		20	25		V
$V_{GD} = V_{BD}$ = −5V, I_D = 10nA	10			10			10			10			20			20			V
V_{GB} = 0V, Source OPEN, I_D = 10nA	15			15			15			15			25			25			V
V_{GB} = 0V, Drain OPEN, I_S = 10µA	15			15			15			15			25			25			V
$V_{GS} = V_{BS}$ = −5V																			
V_{DS} = +10V		1	10		1	10		1	10		1	10							nA
V_{DS} = +20V														1	10		1	10	nA
$V_{GD} = V_{BD}$ = −5V																			
V_{SD} = +10V		1	10		1	10		1	10		1	10							nA
V_{SD} = +20V														1	10		1	10	nA
$V_{DB} = V_{SB}$ = 0V																			
V_{GB} = ±40V			0.1						0.1						0.1				nA
V_{GB} = +25V					10						10								µA
V_{GB} = +30V																	10		µA
$V_{DS} = V_{GS} = V_T$, I_S = 1µA, V_{SB} = 0V	0.5	1.0	2.0	0.5	1.0	2.0	0.1	1.0	2.0	0.1	1.0	2.0	0.1	1.0	2.0	0.1	1.0	2.0	V
V_{DS} = 10V, V_{SB} = 0V, I_D = 20mA, f = 1kHz	10	15		10	15		10	15		10	15		10	15		10	15		mmhos
V_{DS} = 10V, f = 1kHz, $V_{GS} = V_{BS}$ = −15V																			
		2.4	3.5		2.4	3.5		2.4	3.5		2.4	3.5		2.4	3.5		2.4	3.5	pF
		1.3	1.5		1.3	1.5		1.3	1.5		1.3	1.5		1.3	1.5		1.3	1.5	pF
		3.5	4.0		3.5	4.0		3.5	4.0		3.5	4.0		3.5	4.0		3.5	4.0	pF
		0.3	0.5		0.3	0.5		0.3	0.5		0.3	0.5		0.3	0.5		0.3	0.5	pF
I_D = 0.1mA, V_{SB} = 0																			
V_{GS} = +5V		50	70		50	70		50	70		50	70		50	70		50	70	Ω
V_{GS} = +10V		30	45		30	45		30	45		30	45		30	45		30	45	Ω
V_{GS} = +15V		23			23			23			23			23			23		Ω
V_{GS} = +20V		19			19			19			19			19			19		Ω
V_{GS} = +25V		17			17			17			17			17			17		Ω

CHARACTERISTIC CURVES

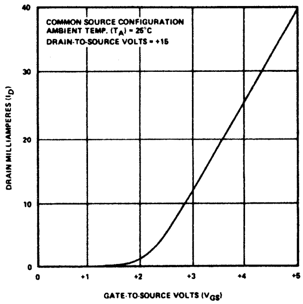
DRAIN CURRENT VS DRAIN-TO-SOURCE VOLTAGE



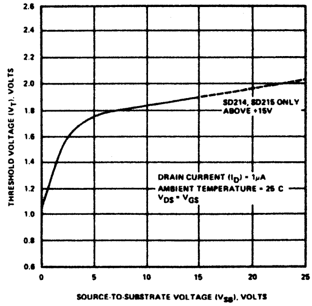
1kHz FORWARD TRANSCONDUCTANCE VS DRAIN CURRENT



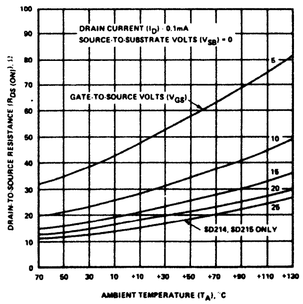
DRAIN CURRENT VS GATE-TO-SOURCE VOLTAGE



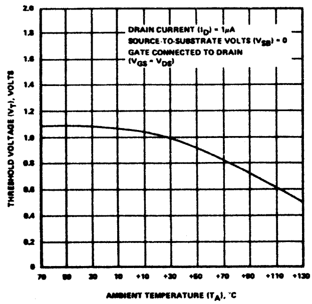
THRESHOLD VOLTAGE VS SOURCE-TO-SUBSTRATE VOLTAGE



DRAIN-TO-SOURCE RESISTANCE VS TEMPERATURE

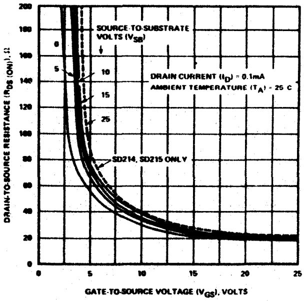


THRESHOLD VOLTAGE VS TEMPERATURE

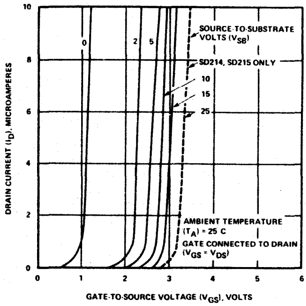


CHARACTERISTIC CURVES (Continued)

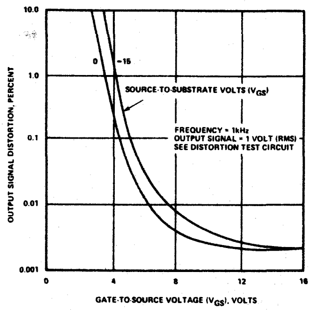
DRAIN-TO-SOURCE RESISTANCE VS GATE-TO-SOURCE VOLTAGE



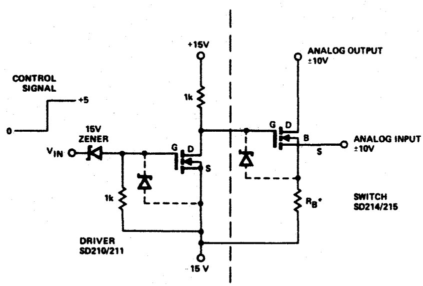
DRAIN CURRENT VS GATE-TO-SOURCE VOLTAGE



DISTORTION VS GATE-TO-SOURCE VOLTAGE



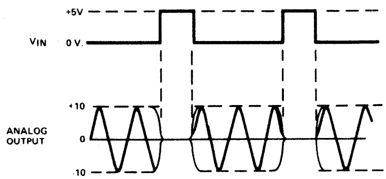
D-MOS DRIVER/SWITCH APPLICATION



R_B* OPTIONAL CURRENT LIMITING RESISTOR

NOTE: ALL RESISTORS STANDARD AND ARE MEASURED IN OHMS.

TYPICAL WAVEFORMS

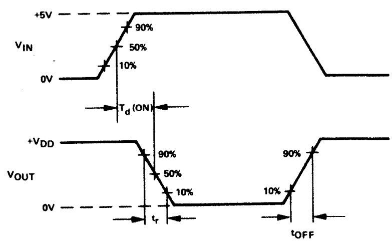


SWITCHING CHARACTERISTICS

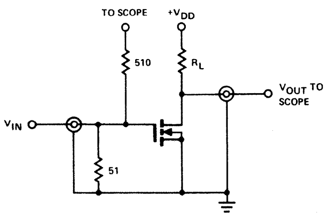
		t_d (ON) (ns)		t_r (ns)		t_{OFF} (ns)	
V_{DD}	R_L	TYP	MAX	TYP	MAX	TYP	MAX
5	680	0.6	1.0	0.7	1.0	9.0	*
10	680	0.7		0.8		9.0	
15	1k	0.9		1.0		14.0	

*t_{OFF} is dependent on R_L and C_L and does not depend on the device characteristics.

SWITCHING WAVEFORMS



TEST CIRCUIT



INPUT PULSE

t_d, t_r < 1ns
PULSE WIDTH = 100ns
REP RATE = 1MHz

SAMPLING SCOPE

t_r < 360ps
R_{IN} = 1MΩ
C_{IN} = 2.0pF

NOTE: ALL RESISTORS STANDARD AND ARE MEASURED IN OHMS.

D-MOS FET DUAL GATE N-CHANNEL ENHANCEMENT
SD300 SD301 SD303 SD304

VHF, UHF AND GENERAL PURPOSE RF APPLICATIONS

DESCRIPTION

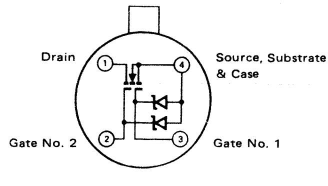
The Signetics D-MOS SD300/301/303/304 are silicon, dual-insulated-gate, field effect transistors of the N-channel enhancement mode type. They are fabricated by the Signetics double-diffused process which gives superior high frequency performance. Zener diodes are connected between the two gates and the substrate. These diodes bypass any voltage transients which lie outside the range of −0.3V to +25.0V. Thus, the gates are protected against damage in all normal handling and operating situations.

The devices' attributes make them ideally suited for a variety of high frequency amplifier and mixer applications. The presence of two gates plus the incorporation of the drift region in the structure, has made the feedback capacity (Crss) less than 0.02pF. A wide AGC capability plus a significant reduction in cross-modulation distortion is now available because of the inherent linearity of these devices. The SD300, 301, 303 and 304 are hermetically sealed in modified 4-lead TO-72 packages.

GENERAL FEATURES

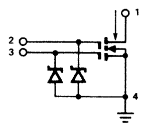
- LOWER CROSS-MODULATION AND WIDER DYNAMIC RANGE THAN BIPOLAR OR SINGLE GATE FETs
- REVERSE AGC CAPABILITY
- LINEAR MIXING CAPABILITY
- DIODE PROTECTED GATES
- HIGH FORWARD TRANSCONDUCTANCE – gfs = 10,000µmhos
- ION-IMPLANTED
- POSITIVE BIAS ONLY

PIN CONFIGURATION (Top View)



Order Part Nos:
SD300DC, SD301DC, SD303DC, SD304DE

DUAL GATE CASCODE BIAS SCHEME



$+V_{DS} = 0 \rightarrow +20$ Volts
$+V_{G1S} = 0 \rightarrow +4$ Volts
$+V_{G2S} = 0 \rightarrow +10$ Volts
$+I_{DS} = 0 \rightarrow +20$mA

FEATURES

PARAMETER	SD300	SD301	SD303	SD304	UNIT
High Gain Through UHF Range	13	14	14		dB at 1GHz
High Gain Through VHF Range				16	dB at 500MHz
Low Noise Through UHF Range	8	6	5.5		dB at 1GHz
Low Noise Through VHF Range				5	dB at 500MHz
Low Input Capacitance	2.0	2.0	3.0	2.5	pF
Low Feedback Capacitance	0.02	0.02	0.02	0.03	pF
Low Output Capacitance	1.0	0.6	0.6	1.0	pF

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C (Unless Otherwise Noted)

Drain-To-Source (V_{DS})
- SD300/304 +25V
- SD301 +20V

DC Gate No. 1-To-Substrate Voltage (V_{G1B}) -0.3V, +10V

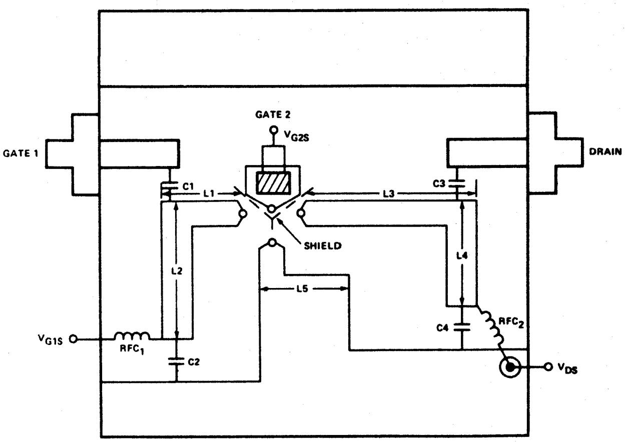
DC Gate No. 2-To-Substrate Voltage (V_{G2B}) -0.3V, +15V

Drain Current (I_D) 50mA

Ambient Temperature Range (T_A)
- Storage -65°C to +175°C
- Operating -65°C to +125°C

Transistor Dissipation (P_T)
- At +25°C Case Temperature 1.2W
  (Derate linearly to +125°C case temperature at the rate of 8.0mW/°C.)
- At +25°C Free-Air Temperature 300mW
  (Derate linearly to +125°C free-air temperature at the rate of 2.0mW/°C.)

TEST FIXTURE (1GHz) (Used With SD300, 301, 303)



DIELECTRIC IS 1/16" TEFLON-FIBERGLASS (3M-K6098-11).
ALL MICROSTRIP WIDTH = 0.175 INCH.

L_1 = 0.42 INCH	C_1 = 0.8-10pF JOHANSON 5201
L_2 = 1.68 INCHES	C_2 = C_4 = 1.20pF JOHANSON 5501
L_3 = 0.64 INCH	C_3 = 0.4-6.0pF JOHANSON 4642
L_4 = 1.52 INCHES	RFC_1 = 0.22μH
L_5 = 0.30 INCH	RFC_2 = 18μH

NOTE: SHIELD AND ALL PASSIVE COMPONENTS ON GROUND PLANE SIDE OF AMPLIFIER.

1000pF BYPASSES ARE:
- DRAIN: CORY FT4-01-2
- GATE 2: AMERICAN TECHNICAL CERAMICS ATC100B (CHIP CAPACITOR)

LAUNCHERS ARE OSM248-2

ELECTRICAL CHARACTERISTICS T_A = +25°C (Unless Otherwise Noted).

PARAMETER		TEST CONDITIONS	SD300			SD301			SD303			SD304			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
BV_{DS}	Drain-To-Source Breakdown Voltage	V_{G1S} = V_{G2S} = 0V, I_D = 5μA	25	30		20	25		20	25		25	30		V
I_{G1SS}	Gate 1 Leakage Current	V_{G1S} = +5V, V_{G2S} = V_{DS} = 0V		0.001	0.1		0.001	0.1		0.001	0.1		0.001	0.1	μA

ELECTRICAL CHARACTERISTICS $T_A = +25°C$ (Unless Otherwise Noted), Continued

PARAMETER		TEST CONDITIONS	SD300			SD301			SD303			SD304			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{G2SS}	Gate 2 Leakage Current	$V_{G2S} = +10V$, $V_{G1S} = V_{DS} = 0V$		0.001	0.1		0.001	0.1		0.001	0.1		0.001	0.1	μA
$I_{D(OFF)}$	Drain-To-Source Leakage Current	$V_{DS} = +15V$, $V_{G1S} = V_{G2S} = 0V$		0.001	1.0		0.001	1.0		0.001	1.0		0.001	1.0	μA
I_{DSS}	Zero Bias Drain Current	$V_{DS} = +15V$, $V_{G1S} = V_{G2S} = 0V$		0.001	1.0		0.001	1.0		0.001	1.0		0.001	1.0	μA
V_{T1}	Gate 1 Threshold Voltage	$V_{DS} = V_{G1S} = V_{T1}$, $V_{G2S} = +10V$, $I_D = 1\mu A$	0.1	1.0	2.0	0.1	1.0	2.0	0.1	0.5	1.5	0.1	1.0	2.0	V
V_{T2}	Gate 2 Threshold Voltage	$V_{DS} = V_{G2S} = V_{T2}$, $V_{G1S} = +4V$, $I_D = 1\mu A$	0.1	1.0	2.0	0.1	1.0	2.0	0.1	0.5	1.5	0.1	1.0	2.0	V
Small Signal Short Circuit Capacitances		f = 1MHz, Gate 2 AC Grounded													
C_{iss}	Input	$V_{DS} = +15V$, $V_{G1S} \cong 3.5V$, $V_{G2S} = +10V$, $I_D = 18mA$		2.0	2.5		2.0	2.5					2.5	3.0	pF
		$V_{DS} = +15V$, $V_{G1S} \cong +2.5V$, $V_{G2S} = +10V$, $I_D = 18mA$ f = 1MHz								3.0	3.5				pF
C_{oss}	Output	$V_{DS} = +15V$, $V_{G1S} = 0V$, $V_{G2S} = +10V$, f = 1MHz		1.0	1.2		0.6	0.8		0.6			1.0	1.2	pF
C_{rss}	Reverse Transfer	$V_{DS} = +15V$, $V_{G1S} = 0V$, $V_{G2S} = +10V$, f = 1MHz		0.02			0.02			0.02			0.03		pF
gfs	Forward Transconductance	$V_{DS} = +15V$, $V_{G1S} \cong +3.5V$ $V_{G2S} = +10V$, $I_D = 18mA$, f = 1kHz	8.0	10.0		8.0	10.0					8.0	10.0		mmhos
		$V_{DS} = +15V$, $V_{G1S} \cong +2.5V$, $V_{G2S} = +10V$, $I_D = 18mA$							13.0	15.0					mmhos
Gps	Power Gain	$V_{DS} = +15V$, $V_{G1S} \cong +3.5V$, $V_{G2S} = +10V$, $I_D = 18mA$													
		f = 1GHz	9.0	13.0*		10.0	14.0*								dB
		f = 500MHz										13.0	16.0		dB
		f = 200MHz	22.0	24.0		22.0	25.0								dB
		$V_{DS} = +15V$, $V_{G1S} \cong +2.5V$, $V_{G2S} = +10V$, $I_D = 18mA$, f = 1GHz							10.0	14.0*					dB
NF	Noise Figure	$V_{DS} = +15V$, $V_{G1S} \cong +3.5V$, $V_{G2S} = +10V$, $I_D = 18mA$													
		f = 1GHz		8.0*	9.0		6.0*	7.0							dB
		f = 500MHz											5.0	6.0	dB
		f = 200MHz		3.0	4.0		2.0	3.0							dB
		$V_{DS} = +15V$, $V_{G1S} \cong +2.5V$, $V_{G2S} = +10V$, $I_D = 18mA$, f = 1GHz								5.5*	7.0				dB
E_{int}	Interfering Signal Level At Gate For 1% Cross-Modulation Distortion. Peak Voltage Referenced To 300Ω System.	$V_{DS} = +15V$, $V_{G2S} = +10V$, $I_D = 18mA$, Desired Signal f = 500MHz, Undesired Signal f = 501MHz		200			200						200		mV
		$V_{DS} = +15V$, $V_{G2S} = +10V$, $I_D = 18mA$, Wanted Signal f = 1GHz, Interfering Signal f = 0.995GHz								150					mV
AGC (V_{G2S})	Range Of Automatic Gain Control	$V_{DS} = +15V$, $V_{G1S} \cong +3.5V$, f = 500MHz		40			40						40		dB
		$V_{DS} = +15V$, $V_{G1S} \cong +2.5V$, f = 500MHz								40					dB
$r_{DS(ON)}$	Drain-To-Source *On Resistance	$V_{G1S} = +5V$, $V_{G2S} = +10V$, $I_D = 0.1mA$		90	130		90	130		65	80		90	130	Ω

*Measured in amplifier test fixture.

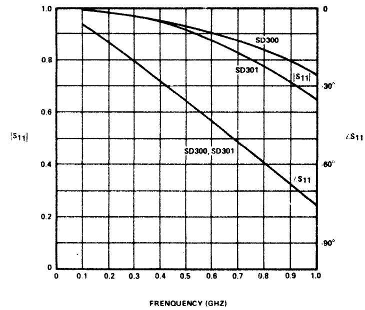
CHARACTERISTIC CURVES

SD300, 301

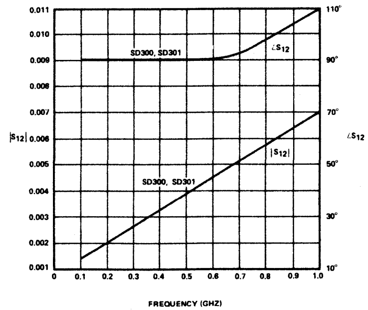
S PARAMETERS

AMBIENT TEMP. (T_A) = +25°C
DRAIN MILLIAMPERES (I_D) = 18
DRAIN-TO-SOURCE VOLTS (V_{DS}) = +15

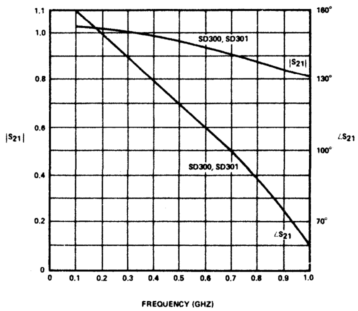
S_{11}



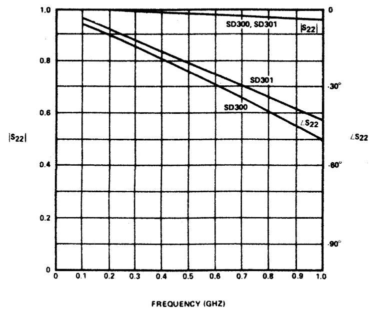
S_{12}



S_{21}



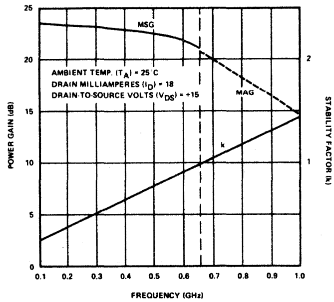
S_{22}



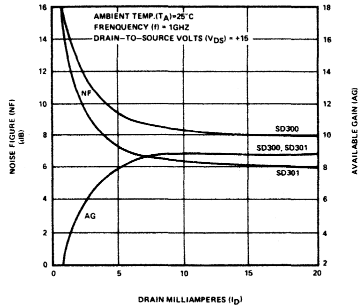
CHARACTERISTIC CURVES (Continued)

SD300, 301

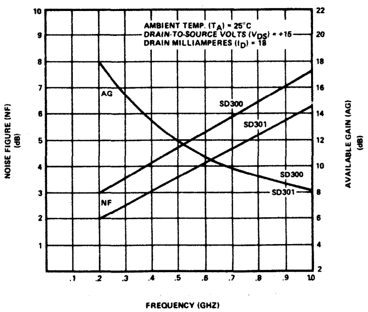
POWER GAIN VS FREQUENCY



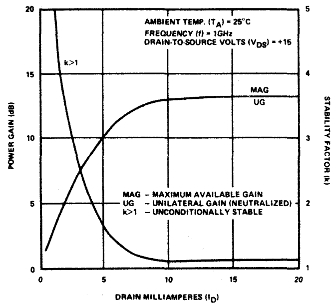
NOISE FIGURE AND AVAILABLE GAIN VS DRAIN CURRENT



NOISE FIGURE AND AVAILABLE GAIN VS FREQUENCY

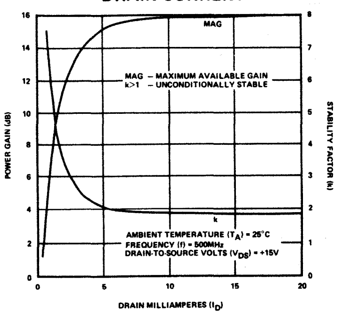


POWER GAIN VS DRAIN CURRENT

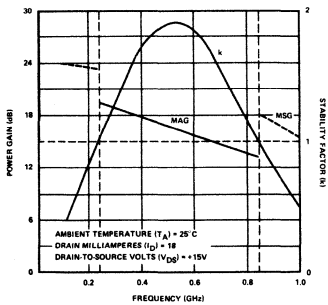


SD304

POWER GAIN VS DRAIN CURRENT



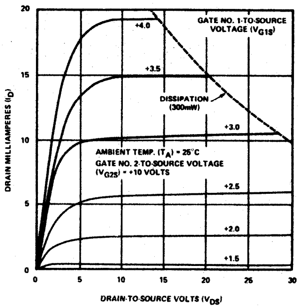
POWER GAIN VS FREQUENCY



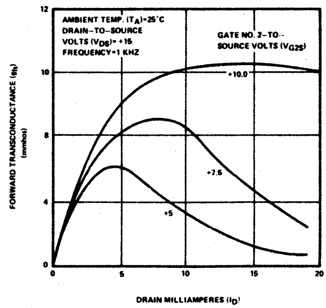
CHARACTERISTIC CURVES (Continued)

SD300, 301, 304

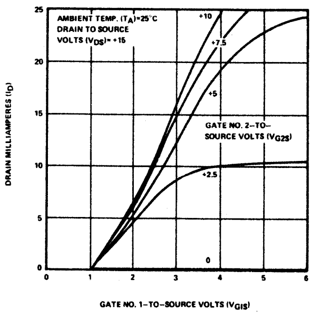
DRAIN CURRENT VS DRAIN-TO-SOURCE VOLTAGE



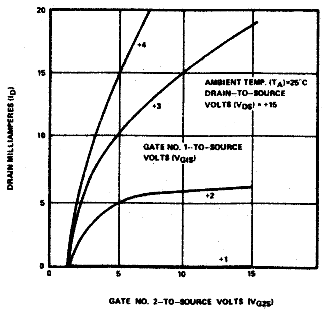
1kHz FORWARD TRANSCONDUCTANCE VS DRAIN CURRENT



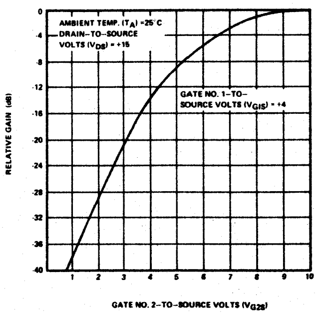
DRAIN CURRENT VS GATE NO. 1-TO-SOURCE VOLTAGE



DRAIN CURRENT VS GATE NO. 2-TO-SOURCE VOLTAGE



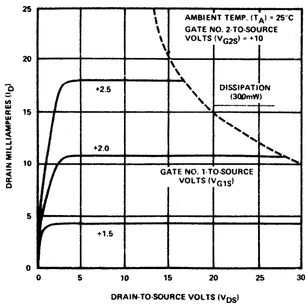
AUTOMATIC GAIN CONTROL RANGE AT 500MHz



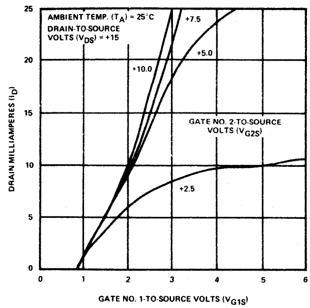
CHARACTERISTIC CURVES (Continued)

SD303

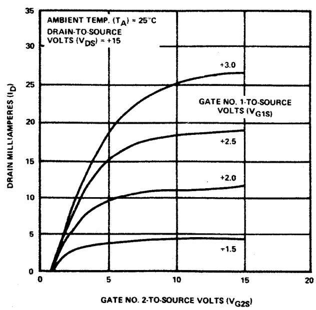
DRAIN CURRENT VERSUS DRAIN-TO-SOURCE VOLTAGE



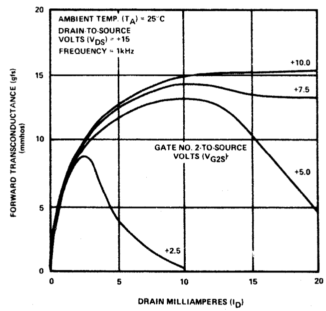
DRAIN CURRENT VERSUS GATE NO. 1-TO-SOURCE VOLTAGE



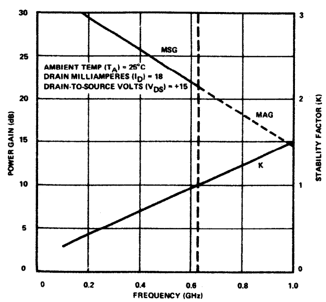
DRAIN CURRENT VERSUS GATE NO. 2-TO-SOURCE VOLTAGE



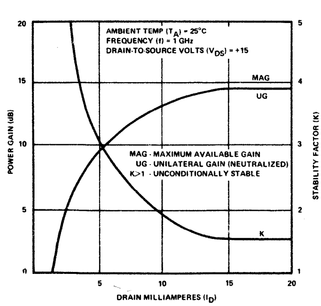
1kHz FORWARD TRANSCONDUCTANCE VERSUS DRAIN CURRENT



POWER GAIN VERSUS FREQUENCY



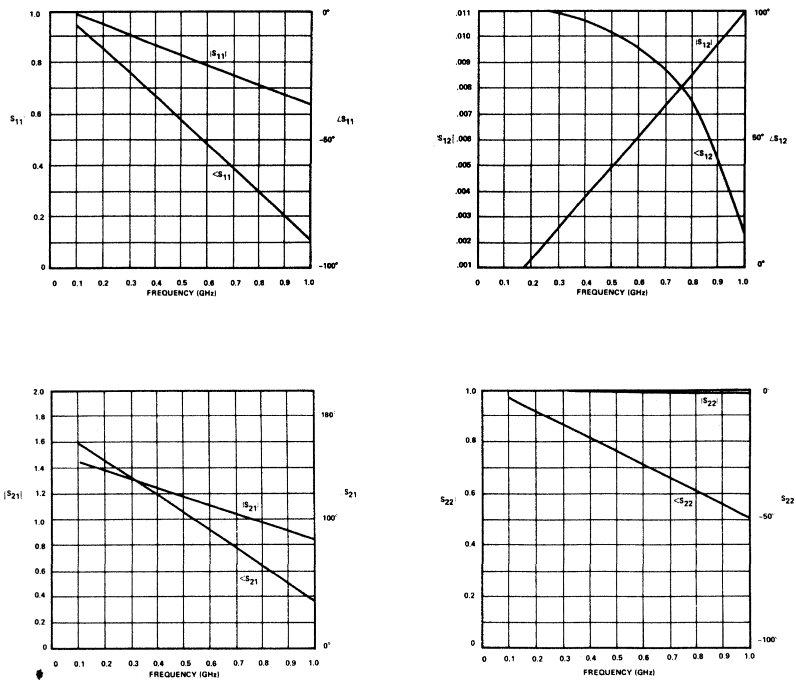
POWER GAIN VERSUS DRAIN CURRENT



CHARACTERISTIC CURVES (Continued)

SD303

S PARAMETERS
AMBIENT TEMP. (T_A) = +25°C
DRAIN MILLIAMPERES (I_D) = 18
DRAIN-TO-SOURCE VOLTS (V_{DS}) = +15

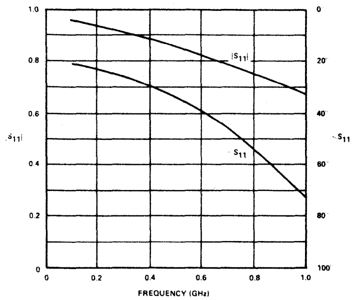


CHARACTERISTIC CURVES (Continued)

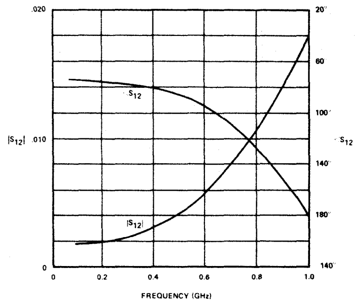
SD304

S PARAMETERS
AMBIENT TEMP. (T_A) = 25°C
DRAIN MILLIAMPERES (I_D) = 18
DRAIN-TO-SOURCE VOLTS (V_{DS}) = +15

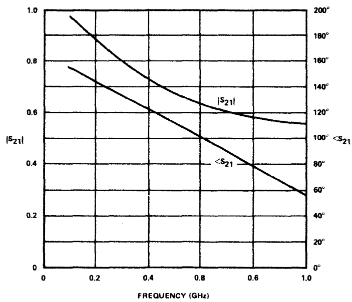
S_{11}



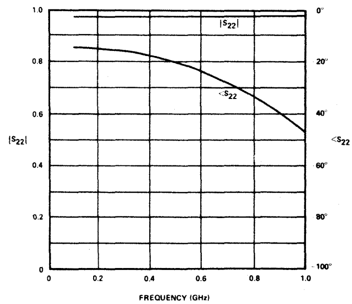
S_{12}



S_{21}



S_{22}



signetics

D-MOS FET - DUAL GATE N-CHANNEL ENHANCEMENT

SD305 SD306

VHF TV AND FM APPLICATIONS

DESCRIPTION

The Signetics D-MOS SD305 and 306 are silicon, dual-insulated gate, field-effect transistors of the N-channel enhancement mode type. Zener diodes are connected between the two gates and the substrate. These diodes bypass any voltage transients which lie outside the range of −0.3V to +20.0V. Thus, the gates are protected against damage in all normal handling and operating situations.

The devices' attributes make them ideally suited for a variety of VHF amplifier and mixer applications. The presence of two gates plus the incorporation of the drift region in the structure has made the feedback capacity (C_{G1D}) typically less than 0.03pF. A wide AGC capability plus significant reduction in cross modulation distortion is now available because of the inherent linearity of the devices. The SD305 and SD306 are hermetically sealed in a 4-lead TO-72 package.

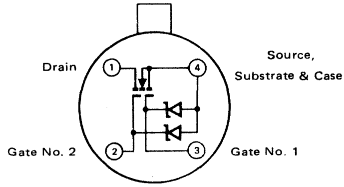
GENERAL FEATURES

- POSITIVE BIAS ONLY
- LOW GATE VOLTAGES
- ENHANCEMENT MODE OPERATION
- WIDE AGC RANGE – 50dB AT 200MHz
- ZENER DIODE GATE PROTECTION
- ION IMPLANTED FOR GREATER RELIABILITY

FEATURES – SD305 (VHF TV and FM Mixer)

- HIGH CONVERSION GAIN – 17dB AT 200MHz WITH $V_{G1S} = V_{G2S}$ FOR BIASING SIMPLICITY

PIN CONFIGURATION (Top View)



ORDER PART NOS. SD305DE and SD306DE

- EXCELLENT ISOLATION FROM GATE NO. 1 (RF) TO GATE NO. 2 (LO) – 20dB AT 200MHz
- LOW INPUT CAPACITANCE – 4.0pF
- LOW FEEDBACK CAPACITANCE – 0.03pF
- EXCELLENT CROSS MODULATION PERFORMANCE AND LOW NOISE OPERATION
- HIGH TRANSCONDUCTANCE – 27mmhos

FEATURES – SD306 (VHF TV and FM RF Amplifier)

- HIGH POWER GAIN WITHOUT NEUTRALIZATION – 20dB AT 200MHz
- LOW NOISE FIGURE – 1.5dB AT 200MHz
- LOW INPUT AND OUTPUT CAPACITANCE – 3.3pF AND 1.0pF CONSTANT WITH AGC
- LOW FEEDBACK CAPACITANCE – 0.03pF
- SUPERIOR CROSS MODULATION PERFORMANCE
- HIGH TRANSCONDUCTANCE – 15mmhos

ABSOLUTE MAXIMUM RATINGS T_A = 25°C (Unless Otherwise Noted)

PARAMETER		SD305	SD306	UNIT
V_{DS}	Drain-To-Source Voltage	+20		V
V_{G1B}	Gate No. 1-To-Substrate Voltage	−0.3 to +20		Vdc
V_{G2B}	Gate No. 2-To-Substrate Voltage	−0.3 to +20		Vdc
I_D	Drain Current	150	50	mA
T_A	Ambient Temperature Range			
	Storage	−65 to +175		°C
	Operating	−65 to +125		°C
P_T	Transistor Dissipation			
	At 25°C Case Temperature	1.2		W
	(Derate linearly to 125°C case temperature at the rate of 8.0mW/°C)			
	At 25°C Free-Air Temperature	300		mW
	(Derate linearly to 125°C free-air temperature at the rate of 2.0mW/°C)			

ELECTRICAL CHARACTERISTICS $T_A = 25°C$

PARAMETER		TEST CONDITIONS	SD305			SD306			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
OFF Characteristics									
BV_{DS}	Drain-To-Source Breakdown Voltage	$V_{G1S} = V_{G2S} = 0V$, $I_D = 5\mu A$	20	30		20	25		V
I_D (OFF)	Drain-To-Source Leakage Current	$V_{DS} = +15V$, $V_{G1S} = V_{G2S} = 0V$		0.001	1.0		0.001	1.0	μA
I_{DSS}	Zero Bias Drain Current	$V_{DS} = +15V$, $V_{G1S} = V_{G2S} = 0V$		0.001	1.0		0.001	1.0	μA
I_{G1SS}	Gate No. 1 Leakage Current	$V_{G1S} = +5V$, $V_{G2S} = V_{DS} = 0V$		0.001	0.1		0.001	0.1	μA
I_{G2SS}	Gate No. 2 Leakage Current	$V_{G2S} = +10V$, $V_{G1S} = V_{DS} = 0V$		0.001	0.1		0.001	0.1	μA
ON Characteristics									
V_{T1}	Gate 1 Threshold Voltage	$V_{DS} = V_{G1S} = V_{T1}$, $V_{G2S} = +10V$, $I_D = 1\mu A$	0.1	1.0	2.0	0.1	0.5	1.5	V
V_{T2}	Gate 2 Threshold Voltage	$V_{DS} = V_{G2S} = V_{T2}$, $V_{G1S} = +5V$, $I_D = 1\mu A$	0.1	1.0	2.0	0.1	0.5	1.5	V
r_{DS} (ON)	Drain-To-Source On Resistance	$V_{G1S} = +5V$, $V_{G2S} = +10V$, $I_D = 0.1mA$		30	60		65	100	Ω
Small Signal Characteristics									
gfs	Forward Transconductance	$V_{DS} = +15V$, $V_{G2S} = +10V$, f = 1kHz							
		$I_D = 50mA$	24	27					mmhos
		$I_D = 18mA$				13	15		mmhos
gfs (CONV)	Conversion Transconductance	$V_{DS} = +15V$, $V_{G1S} = V_{G2S}$, $I_D = 8mA$, f = 1kHz, E_{LO} (RMS) = 750mV		10					mmhos
Capacitances		f = 1MHz, Gate 2 AC Grounded							
C_{G1S}	Input	$V_{DS} = +15V$, $V_{G2S} = +10V$							
		$I_D = 50mA$		4.0	5.0				pF
		$I_D = 18mA$					3.3	3.6	pF
		$V_{DS} = +15V$, $V_{G1S} = V_{G2S}$, $I_D = 8mA$		4.0	5.0				pF
C_{DS}	Output	$V_{DS} = +15V$, $V_{G1S} = 0V$, $V_{G2S} = +10V$		1.3	1.7		1.0	1.3	pF
C_{G1D}	Reverse Transfer	$V_{DS} = +15V$, $V_{G1S} = 0V$, $V_{G2S} = +10V$		0.03			0.03		pF
Input Admittance		f = 200MHz, $V_{DS} = +15V$	$V_{G1S} = V_{G2S}$, $I_D = 8mA$			$V_{G2S} = +10V$, $I_D = 18mA$			mmhos
	Re (y_{11})		1.05			1.11			
	Im (y_{11})		6.66			4.76			
Output Admittance									
	Re (y_{22})		0.73			1.05			
	Im (y_{22})		2.09			1.54			

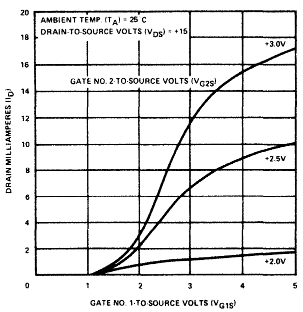
ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$

PARAMETER	TEST CONDITIONS	SD305			SD306			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Forward Transmittance Re (y_{21}) Im (y_{21})			4.69 -3.01			13.23 -5.62		
Reverse Transmittance Re (y_{12}) Im (y_{12})			0.04 -0.03			0.01 -0.04		mmhos
G_{PS} Power Gain[2]	$V_{DS} = +15V$, $V_{G2S} = +10V$, $I_D = 18mA$, f = 200MHz				17	20		dB
$G_{PS\ (CONV)}$ Conversion Power Gain[1]	$V_{DS} = +15V$, $V_{G1S} = V_{G2S}$, $I_D = 8mA$, $f_{rf} = 200MHz$, $f_{LO} = 245MHz$	14	17					dB
NF Noise Figure	$V_{DS} = +15V$, $V_{G2S} = +10V$, $I_D = 18mA$, f = 200MHz					1.5	2.5	dB
AGC_{VG2S} Range Of Automatic Gain Control	$V_{DS} = +15V$, $V_{G1S} \cong +2.5V$, $V_{G2S} = +10V \rightarrow 0V$, f = 200MHz					50		dB
E_{INT} Interfering Signal Level At Gate 1 For 1% Cross Modulation Distortion, Peak Voltage Referenced To 50Ω System[3]	$V_{DS} = +15V$, $V_{G2S} = +8V$, $I_D = 15mA$, Wanted signal f = 200MHz Interfering signal f = 196MHz					480		mV

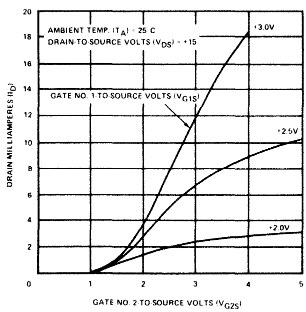
NOTES:
1. Measured in mixer test fixture.
2. Measured in amplifier test fixture.
3. Measured as shown in block diagram.

SD305 CHARACTERISTIC CURVES

DRAIN CURRENT VS GATE NO. 1-TO-SOURCE VOLTAGE

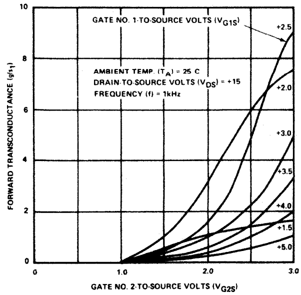


DRAIN CURRENT VS GATE NO. 2-TO-SOURCE VOLTAGE

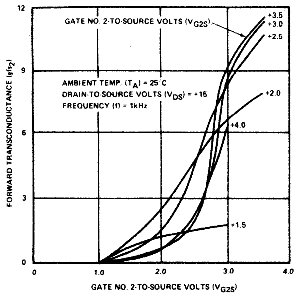


SD305 CHARACTERISTIC CURVES (Continued)

GATE NO. 1 FORWARD TRANSCONDUCTANCE VS GATE NO. 2-TO-SOURCE VOLTAGE



GATE NO. 2 FORWARD TRANSCONDUCTANCE VS GATE NO. 1-TO-SOURCE VOLTAGE

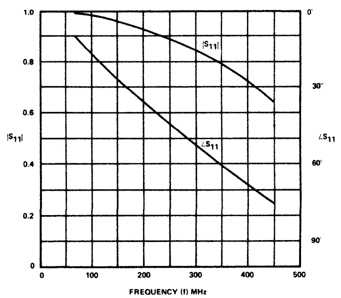


S PARAMETERS

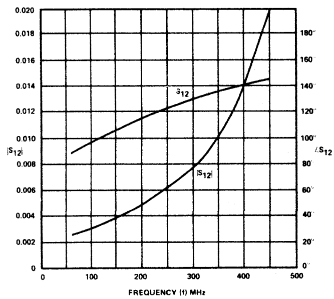
AMBIENT TEMP. (T_A) = +25°C
DRAIN-TO-SOURCE VOLTS (V_{DS}) = +15

DRAIN MILLIAMPERES (I_D) = 8
GATE NO. 1-TO-SOURCE VOLTS = GATE NO. 2-TO-SOURCE VOLTS

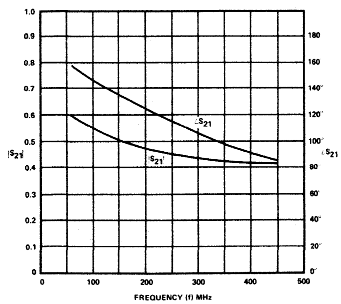
S_{11}



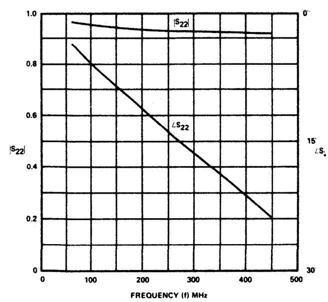
S_{12}



S_{21}

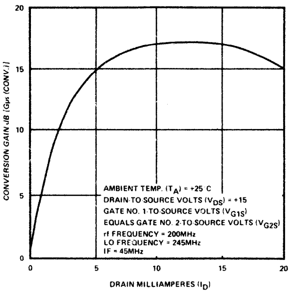


S_{22}

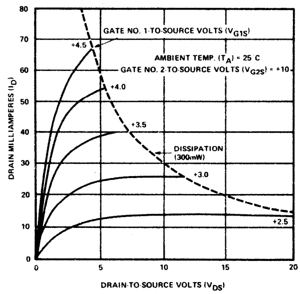


SD305 CHARACTERISTIC CURVES (Continued)

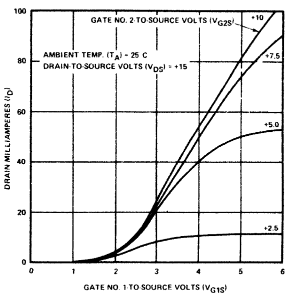
CONVERSION GAIN VS DRAIN CURRENT



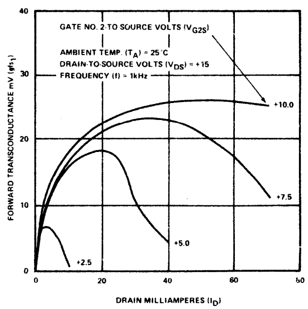
DRAIN CURRENT VS DRAIN-TO-SOURCE VOLTAGE



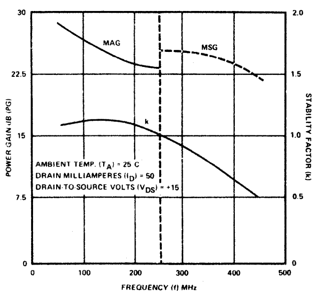
DRAIN CURRENT VS GATE NO. 1-TO-SOURCE VOLTAGE



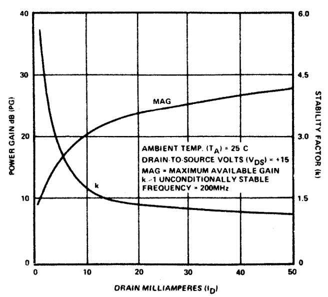
GATE NO. 1 FORWARD TRANSCONDUCTANCE VS DRAIN CURRENT



POWER GAIN VS FREQUENCY

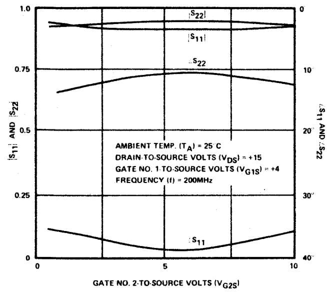


POWER GAIN VS DRAIN CURRENT

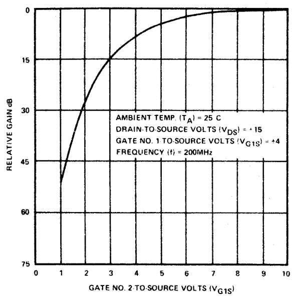


SD305 CHARACTERISTIC CURVES (Continued)

AUTOMATIC GAIN CONTROL VS S_{11} AND S_{22}



AUTOMATIC GAIN CONTROL RANGE

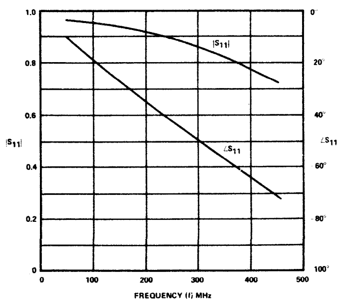


S PARAMETERS

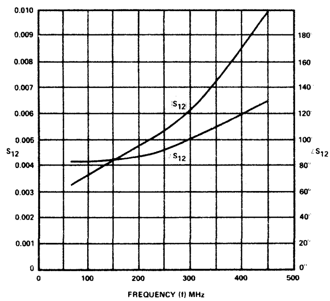
AMBIENT TEMP. $(T_A) = +25°C$
DRAIN-TO-SOURCE VOLTS $(V_{DS}) = +15$

DRAIN MILLIAMPERES $(I_D) = 50$
GATE NO. 1-TO-SOURCE VOLTS = GATE NO. 2-TO-SOURCE VOLTS

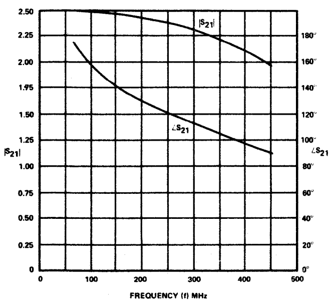
S_{11}



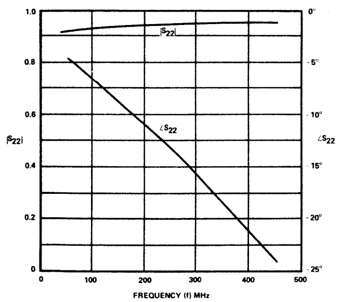
S_{12}



S_{21}

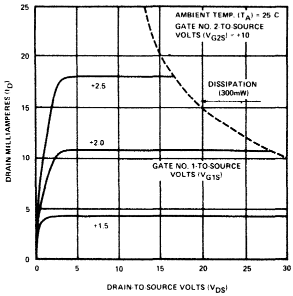


S_{22}

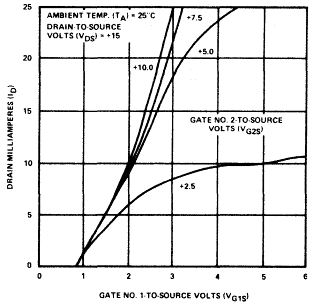


SD306 CHARACTERISTIC CURVES

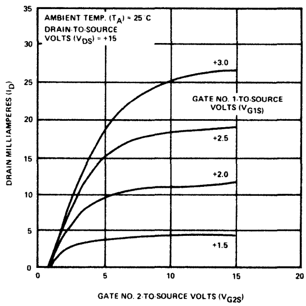
DRAIN CURRENT VS DRAIN-TO-SOURCE VOLTAGE



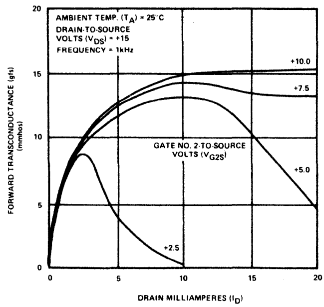
DRAIN CURRENT VS GATE NO. 1-TO-SOURCE VOLTAGE



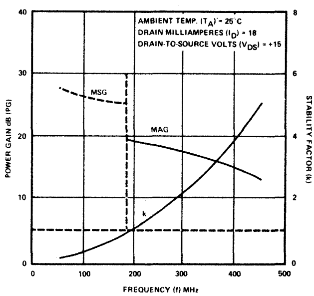
DRAIN CURRENT VS GATE NO. 2-TO-SOURCE VOLTAGE



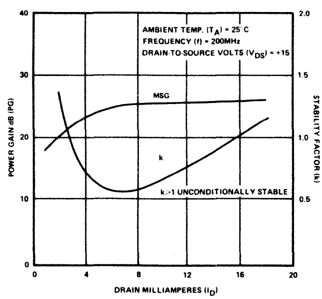
1kHz FORWARD TRANSCONDUCTANCE VS DRAIN CURRENT



POWER GAIN VS FREQUENCY

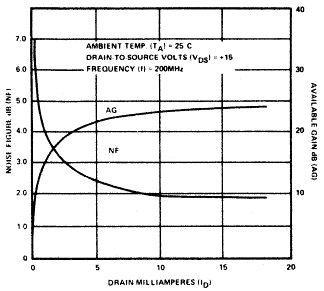


POWER GAIN VS DRAIN MILLIAMPERES

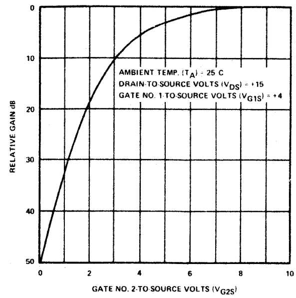


SD306 CHARACTERISTIC CURVES (Continued)

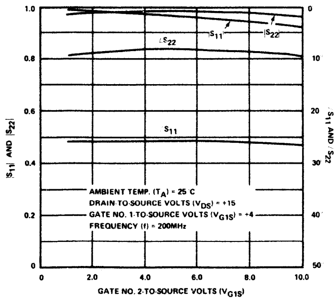
NOISE FIGURE AND AVAILABLE GAIN VS DRAIN CURRENT



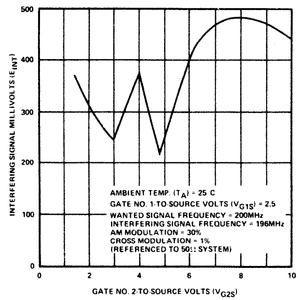
AUTOMATIC GAIN CONTROL RANGE AT 200MHz



S_{11} AND S_{22} VS AUTOMATIC GAIN CONTROL



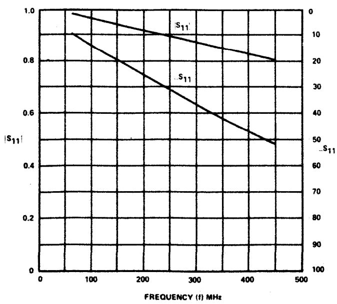
INTERFERING SIGNAL LEVEL VS GATE NO. 2-TO-SOURCE VOLTS



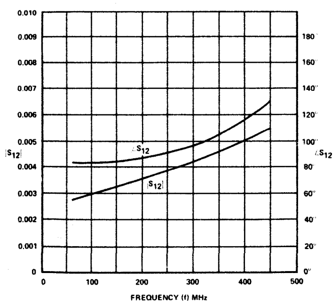
S PARAMETERS

AMBIENT TEMP. (T_A) = +25°C
DRAIN MILLIAMPERES (I_D) = 18
DRAIN-TO-SOURCE VOLTS (V_{DS}) = 15

S_{11}

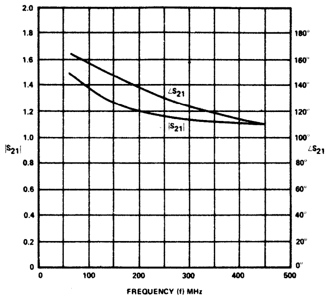


S_{12}

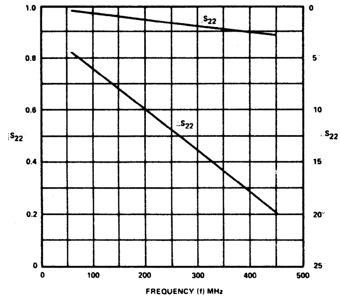


SD306 CHARACTERISTIC CURVES (Continued)

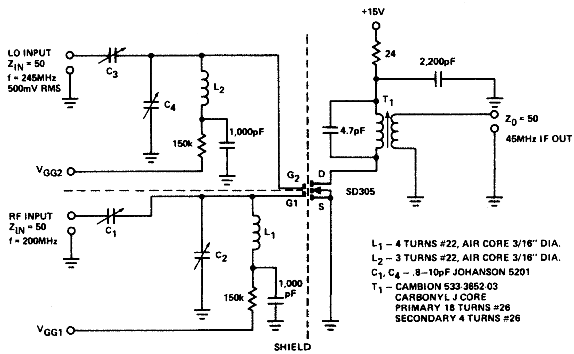
S_{21}



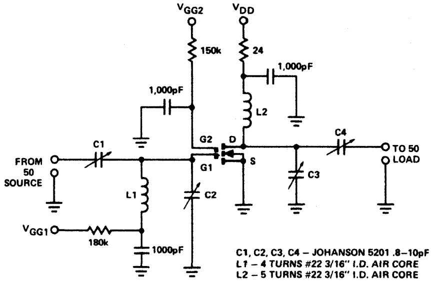
S_{22}



TEST CIRCUITS



SD305 200MHz/45MHz MIXER TEST CIRCUIT

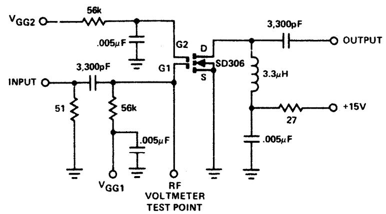


SD306 200MHz TEST AMPLIFIER; POWER GAIN, NOISE FIGURE

SD306
TEST PROCEDURE FOR CROSS MODULATION DISTORTION MEASUREMENTS

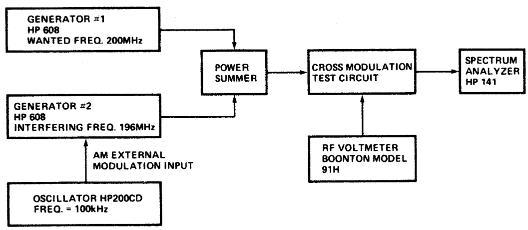
1. Modulation on Generator #2 is set at 100kHz, 30% AM modulation (sidebands down 15.6dB) with an output signal frequency equal to 196MHz.
2. Generator #2 is set at approximately −15dbm, 200MHz.
3. While observing the test circuit output spectrum, adjust the signal level of the interfering frequency so that the sidebands on the desired frequency are 46dB down from the carrier. This corresponds to 1% cross modulation.
4. Turn off Generator #1 and turn off the modulation on Generator #2.
5. Using the RF voltmeter, measure the amplitude of the interfering signal at the test point.

TEST CIRCUIT



SD306 CROSS MODULATION TEST CIRCUIT

BLOCK DIAGRAM OF CROSS MODULATION TEST



NOTES

signetics

APPLICATIONS MEMO SD305 SD306

A VOLTAGE TUNED VHF TV TUNER

SYSTEM DESIGN

Television set manufacturers generally specify the requirements for tuners to be incorporated in their sets. The familiar turret tuner has served the industry and the consumer well over the past years. However, these tuners have an inherent disadvantage in that the contacts become dirty and worn resulting in an expensive service call and subsequent customer dissatisfaction. The advent of the voltage variable semiconductor capacitor now makes it feasible and economically possible to produce a contactless all solid state television tuner.

Set manufacturers generally require about 30dB overall gain with AGC gain reductions to 50dB. Acceptable noise figures range from 3 to 8dB. Cross modulation performance has also recently been of greater concern particularly in regard to what is known as the channel 6 color beat. Image and IF rejection specifications are also strictly adhered to. Some other requirements in regard to oscillator radiation are controlled by the FCC. These and others to be made evident requirements are met for a VVC VHF tuner by the following design:

ANTENNA FILTER

To improve crossmodulation, image and IF rejection performance an RF antenna filter is included. This consists of two cascaded filters: one a band stop filter to attenuate the FM band, the other a high pass with cut-off just below channel 2. This filter is shown in Figure 1 and consists of C3 through C9 and L1 through L6. It may easily be designed from handbook formulas.

SCHEMATIC DIAGRAM

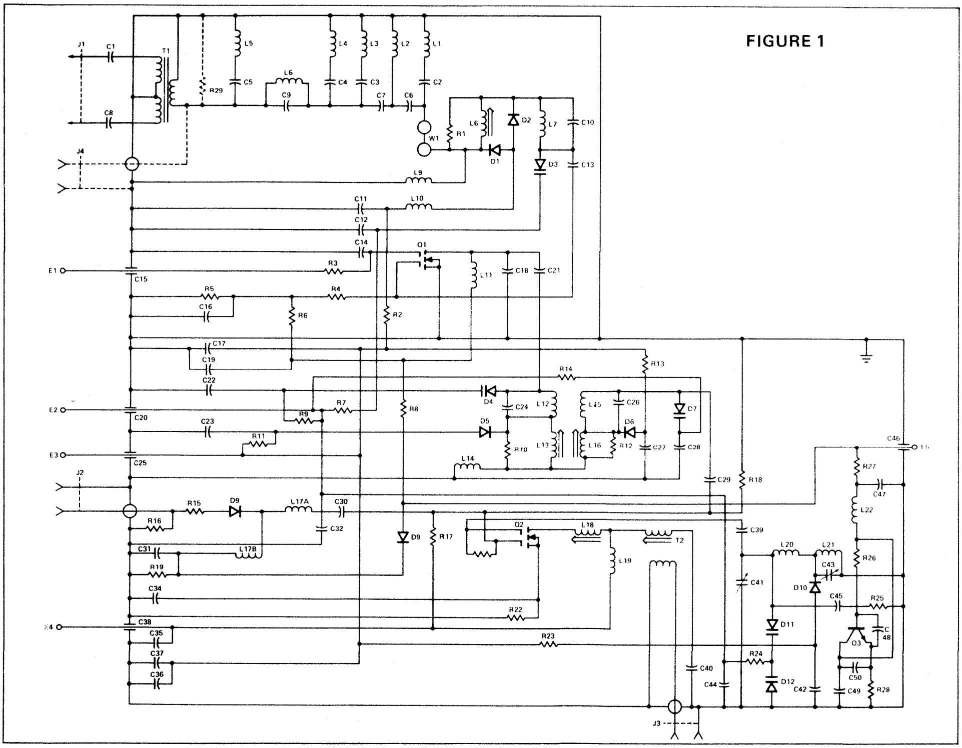


FIGURE 1

SYSTEM DESIGN (Continued)

RF STAGE

From an economic standpoint, it is possible to use only one active device in this stage. Therefore a device giving large RF gain is sought as a primary requirement. If the device itself has a low noise figure, the large gain it offers will overcome the generally poor noise figure of the subsequent mixer stage. AGC voltage will be applied only to the RF stage. A desirable feature here is that the AGC voltage remain unipolar, that is, the voltage should not cross zero anywhere in the controlled range. The Signetics SD306 is an admirable performer in this regard.

An impedance matching network is required following the 75 ohm antenna filter. This provides a conjugate match to the input impedance at gate 1 of the dual gate MOS FET. The network is electronically tuned by a voltage variable capacitor to maintain the matched condition for each channel. Since the capacitance range of the varactor (VVC), D3 in Figure 1 is limited, the entire VHF band cannot be tuned. Therefore an electrically controlled band switch is used and the matching network is divided. In Figure 1, pin diodes D1 and D2 short circuit L8 and place L10 in parallel with L9 for the high band. For the low band L7 is in series with L8 and L10 is not connected when the diodes are nonconducting.

Adequate bypassing of a source resistor in the usual RF amplifier is always an attendant problem especially on a printed circuit layout. The design of the SD306 allows the omission of the source resistor and its bypass. The source terminal of this FET may therefore be directly grounded for minimum undesirable feedback impedance.

INTERSTAGE

The interstage provides the greatest selectivity since it consists of a double tuned network. The low band network contains a complex coupling scheme to control bandwidth as the circuit is tuned. The coupling consists of L14 in Figure 1 and the stray capacitance between the primary and secondary coils and printed wiring. This results in nearly constant bandwidth over the entire low band but the degree of overcoupling varies as shown in Figure 2, the RF interstage responses. This however is not detremental since the single tuned antenna circuit response will fill this in as shown in Figure 3, the overall RF responses.

Diodes D5 and D6 form a bandswitch which short the low band coils, L13, L14, and L16 and leave the high band coils, L12 and L15 active. The mutual coupling in this case is largely electromagnetic. The high band RF responses are also shown in Figures 2 and 3.

MIXER – IF AMPLIFIER

The mixer for this design has an additional function in that it must serve as an IF amplifier for the companion UHF tuner. The biasing arrangement is therefore a compromise between best operation as a mixer and a straight IF amplifier. When gate 2 is used for oscillator injection, the differences in biasing between the two modes of operation are not large. When gate 2 is used for oscillator injection, two additional performance advantages are realized. One is that the bias for the device is simplified because gate 1 and gate 2 can be at the same potential. The other advantage is that there will be greater than 20dB isolation between the local oscillator and the RF input. This minimizes LO radiation out of the antenna terminals.

The UHF IF input circuit is a double tuned "low side C" scheme where L17A in Figure 1 is one coil while the other is located in the UHF tuner. The coupling capacitor consists partly of the interconnecting coaxial cable. This circuit is detuned when UHF is not used by diode D9 and L17B.

The mixer output circuit is also a double tuned network for increased selectivity to reject oscillator frequency especially on the low frequency channels.

OSCILLATOR

The use of a dual gate MOS FET as mixer for improved crossmodulation characteristics usually requires large oscillator voltage swings to achieve efficient mixing action. A bipolar mixer will need 100 to 200 millivolts injection compared to 1 to 3 volts injection for a typical dual gate MOS FET. This requirement is overcome by using the SD305 which requires only 500mV injection.

The oscillator design is a straightforward ordinary common collector Colpitts type. The oscillator tuning diodes are placed back-to-back to cancel some inherent nonlinearities associated with their large signal operation. Oscillator tracking is achieved by use of only trimmer capacitors in both bands. The low band tracking could be improved with the addition of a padder capacitor but this requires a trimmer of value less than the stray capacitance in the circuit and is therefore not feasible. The RF bandwidth has been made sufficiently broad in the low band to accomodate the tracking error.

SCHEMATIC DIAGRAM

Figure 1 is the schematic diagram of the complete voltage variable capacitor VHF television tuner. Shown at the left hand side are two alternate modes of input connection, either 300 ohm balanced or 75 ohm unbalanced. This is followed by the antenna input filter, the input matching network, and the active device. These elements comprise the first shielded compartment of the tuner. The second compartment contains only the double tuned interstage network and the input network for the IF of the UHF companion tuner. The third compartment contains the mixer and local oscillator. The IF output is taken from this compartment.

CONNECTOR AND TERMINAL DESIGNATIONS

Item	Description
E1	AGC terminal. 0-10 VDC. Max. gain at 10 VDC.
E2	Tuning Voltage Terminal, 2-25 VDC.

CONNECTOR AND TERMINAL DESIGNATIONS
(Continued)

Item	Description
E3	Band Switch Terminal, low band −2 to −20 VDC, high band +20 VDC.
E4	Mixer B+ terminal, +20 VDC.
E5	RF and Local Oscillator B+ Terminal, +20 VDC.
J1	300 ohm balanced line antenna input terminal.
J2	UHF Tuner IF Input Terminal.
J3	43.5 MHz IF Output Terminal.
J4	75 ohm unbalanced Line Antenna Input Terminal (optional).

ALIGNMENT

Except for the oscillator, on variable trimmer capacitors have been used in the RF circuits of this design. In a printed circuit design the stray capacitances due to the wiring do not vary much between units, the VVC's are purchased in matched sets, and the interelectrode capacitances of the active devices are only a fraction of the total shunt circuit capacity. The active device capacitance variations between units would be the only reason for the use of trimmers and since this is only a fraction of the total any resulting detuning will be small and can be compensated by the variation of the inductors.

ANTENNA FILTER ALIGNMENT

All components of this filter are mounted on the same printed circuit as the tuner components. To accurately align this filter, it must not be connected as its output to any tuner component. Therefore a jumper wire replaces a connection on the printed circuit. This jumper is replaced after alignment of the filter. The filter is aligned with sweep frequency techniques using appropriate marker frequencies.

The turns of free standing coils are separated as appropriate to affect tuning of each filter element. The coils are initially wound for slightly too large an inductance.

INTERSTAGE FILTER ALIGNMENT

It is generally necessary to align the interstage before the input matching network. The input network is swamped with a low value resistance so that it does not effect the interstage response. The mixer output circuit is also similarly swamped. The RF response is then viewed with sweep frequency techniques using the mixer source terminal as a connection point to the vertical amplifier of the oscilloscope. Responses as shown in Figure 2 should be achieved. The low band coils are provided with adjustable cores while the high band adjustments are made by pushing the coil turns.

INPUT MATCHING NETWORK

Removal of the input swamping resistor will allow this network to be tracked to the interstage response achieved above. The results as shown in Figure 3 should be achieved.

MIXER OUTPUT CIRCUIT

In this case the interstage network is swamped with a resistance and the IF alignment frequency is introduced across the interstage network. The output swamping resistor used in the above alignment is removed from the IF output network and this circuit is aligned to a maximally flat response at the IF frequency. The IF output terminal is used as a point of measurement in this case.

OSCILLATOR TRACKING

The oscillator is made to track the RF circuits just aligned by adjusting the L-C ratio so that the oscillator is exactly 43.5 MHz above the RF at the end channels of both bands. This results in a small deviation in the band centers, but the RF bandwidths are sufficiently broad to accommodate this error. The overall responses should appear as shown in Figure 4.

PERFORMANCE

The essential performance characteristics are tabulated below. This data was taken for a tuner which used the SD304 for the RF amplifier and mixer. The tuner was later modified to use the SD305 and SD306. Complete data has not been completed at the present time. However, a preliminary look showed a 3-4dB improvement in gain and a

Channel	Gain	Gain*	NF	NF*	VSWR	V_{tune}	Gain Red.	Image Rej.
2	31.5		5.2		2.1	2.50	66	70
3	31	33	4.8	2.9	1.9	4.22	65.5	70
4	32		4.7		2.3	5.96	64	70
5	31.5		4.8		1.9	11.15	63	70
6	31		4.8		1.7	23.5	61.5	70
7	26		5.1		2.1	6.28	60	70
8	26.5		4.9		2.3	7.34	58	65
9	27		4.7		2.1	8.52	56.5	64
10	27		4.6		1.9	9.98	56	61
11	27		4.7		1.9	12.07	55	63
12	27.5	30	4.6	4.0	1.9	15.58	54.5	65
13	27.5		4.8		1.9	24.0	54	65

*SD305/306 Tuner.

PERFORMANCE (Continued)

1-2dB reduction in noise figure. A preliminary look at crossmodulation for the channel 6 color beat indicated it to be 60dB down for an input level of one millivolt for each of the channel 6 carriers. Input VSWR was somewhat in excess of 3 with the input circuit as shown in Figure 1. This is partly due to oscillator mistracking in the low band. Since the schematic was drawn a damping resistor of 3.3k was added across L8 to reduce the VSWR to the figures in the tabulation.

CONSTRUCTION

The tuner chassis consists mechanically of a one inch wide strip of sheet metal formed into a U-shaped frame with ears bent outwardly. The ears serve as a mounting base. Phono jack connectors are soldered into appropriate holds on this frame and are connected to respective points on the printed circuit board. The open end of the U-shaped frame is closed with another one inch flat strip soldered at its ends to the U-frame. This strip contains the five feedthrough capacitors which form the external connection points.

The printed circuit board rests on kicked out tabs of the frame and is soldered to the inside wall of the frame at several places around the periphery. Two shields separate the various stages and provide ground connections to several points on the printed circuit which would be inaccessible otherwise. To avoid making each of the shields of two pieces, one for each side of the printed circuit board, long tabs of a one piece shield extend through slots in the board to contact the cover on one side while the opposite end of the shield contacts the cover on the other side. The covers are made with fingers bent at greater than a right angle all along the edge of the cover.

PARTS LIST

CAPACITORS

Item	Value	Description	Lead Spacing	Mepco/Electra #	Standard #
C1	450 pF	Ceramic Disc	0.25″	na	
C2	450	Ceramic Disc	0.25	na	
C3	3.9	Ceramic Plate	0.1	2222 641 09398	
C4	56	Ceramic Plate	0.1	2222 641 10569	
C5	3.9	Ceramic Plate	0.1	2222 641 09398	
C6	27	Ceramic Plate	0.1	2222 641 10279	
C7	27	Ceramic Plate	0.1	2222 641 10279	
C8	27	Ceramic Plate	0.1	2222 641 10279	
C9	27	Ceramic Plate	0.1	2222 641 10279	
C10	1,000	Ceramic Plate	0.1	2222 629 05102	
C11	3.9	Ceramic Plate	0.1	2222 641 09398	
C12	1,000	Ceramic Plate	0.1	2222 629 05102	
C13	1,000	Ceramic Plate	0.1	2222 629 05102	
C14	1,000	Ceramic Plate	0.1	2222 629 05102	
C15	1,000	Ceramic Plate	0.2	2222 629 06102	
C16	1,000	Ceramic Plate	0.1	2222 629 05102	
C17	1,000	Ceramic Feedthru	–	na	
C18	1,000	Ceramic Plate	0.1	2222 629 05102	
C19	1	Ceramic Plate	0.1	2222 641 03108	
C20	1,000	Ceramic Plate	0.2	2222 629 06102	
C21	1,000	Ceramic Plate	0.2	2222 629 06102	
C22	1,000	Ceramic Plate	0.2	2222 629 06102	
C23	1,000	Ceramic Feedthru	–	na	
C24	3.3	Ceramic Plate	0.1	2222 641 09338	
C25	1.8	Ceramic Plate	0.1	2222 641 03188	
C26	1,000	Ceramic Feedthru	–	na	
C27	1,000	Ceramic Plate	0.2	2222 629 06102	
C28	1,000	Ceramic Plate	0.2	2222 629 06102	
C29	8.2	Ceramic Plate	0.2	2222 642 09828	
C30	22	Ceramic Plate	0.1	2222 641 10229	
C31	4,700	Ceramic Plate	0.1	2222 629 05472	
C32	4,700	Ceramic Plate	0.2	2222 629 06472	
C33	4,700	Ceramic Plate	0.1	2222 629 05472	
C34	1,000	Ceramic Plate	0.1	2222 629 05102	
C35	1.5	Ceramic Plate	0.1	2222 641 03158	

PARTS LIST (Continued)

CAPACITORS

Item	Value	Description	Lead Spacing	Mepco/Electra #	Standard #
C36	1pF	Ceramic Plate	0.1″	2222 641 03108	
C37	10,000	Ceramic Plate	0.1	2222 629 05103	
C38	1,000	Ceramic Plate	0.2	2222 629 06102	
C39	1,000	Ceramic Feedthru	–	na	
C40	0.5-3	Ceramic Tubular Trimmer		na	
C41	1,000	Ceramic Plate	0.1	2222 629 05102	
C42	1,000	Ceramic Plate	0.1	2222 629 05102	
C43	0.5-3	Ceramic Tubular Trimmer		na	
C44	2.7	Ceramic Plate	0.1	2222 641 09278	
C45	1,000	Ceramic Plate	0.1	2222 629 05102	
C46	1,000	Ceramic Feedthru	–	na	
C47	10	Ceramic Plate	0.1	2222 641 10109	
C48	1,000	Ceramic Plate	0.2	2222 629 06102	
C49	1,000	Ceramic Plate	0.1	2222 629 05102	
C50	8.2	Ceramic Plate	0.1	2222 641 09828	

CHOKES AND COILS

Item	# Turns	Winding Direc.	Wire No.	I.D.	Coil Form	Core
L1	13 1/2	L	26	0.213″	na	na
L2	3 1/2	R	24	0.130	na	na
L3	13 1/2	L	26	0.213	na	na
L4	10 1/2	R	26	0.213	na	na
L5	7 1/2	L	24	0.150	na	na
L6	10 1/2	R	26	0.213	na	na
L7	3 1/2	R	24	0.130	na	na
L8	8 1/2	R	24	–	0.166 O.D. paper	J, 6-32 X 1/4
L9	7 1/2	L	24	0.150	na	na
L10	2 1/2	R	24	0.130	na	na
L11	30	L	34 NY CEL	0.156	na	na
L12	3 1/2	L	22	0.150	na	na
L13	11 1/2	R	24	–	0.166 O.D. paper	J, 6-32 X 1/4
L14	4 1/2	L	24	0.150	na	na
L15	3 1/2	R	22	0.150	na	na
L16	8 1/2	L	24	–	0.166 O.D. paper	J, 6-32 X 1/4
L17A	12 1/2	R	34	–	0.25 O.D. polyprop	J, 10-32 X 5/16
L17B	12 1/2	R	34	–	On same form at opposite end	
L18	25	R	30	–	0.25 O.D. polyprop	J, 10-32 X 5/16
L19	15 1/2	L	26	0.166	na	na
L20	3 1/2	L	24	0.150	na	na
L21	6 1/2	R	24	–	0.166 O.D. paper	J, 6-32 X 1/4
L22	30	L	34 NY CEL	0.156	na	na

TRANSFORMERS

T1 300 ohm balanced to 75 ohm unbalanced trifilar wire on small toroidal core
(details not available at this time)

T2	25 (pri.)	L	30	–	0.25 O.D. polyprop	J, 10-32 X 5/16
	3 (sec.)	R	28	–	(Wound over cold side of primary)	

PARTS LIST (Continued)

RESISTORS

All resistors are 1/4 watt carbon composition of carbon film types.

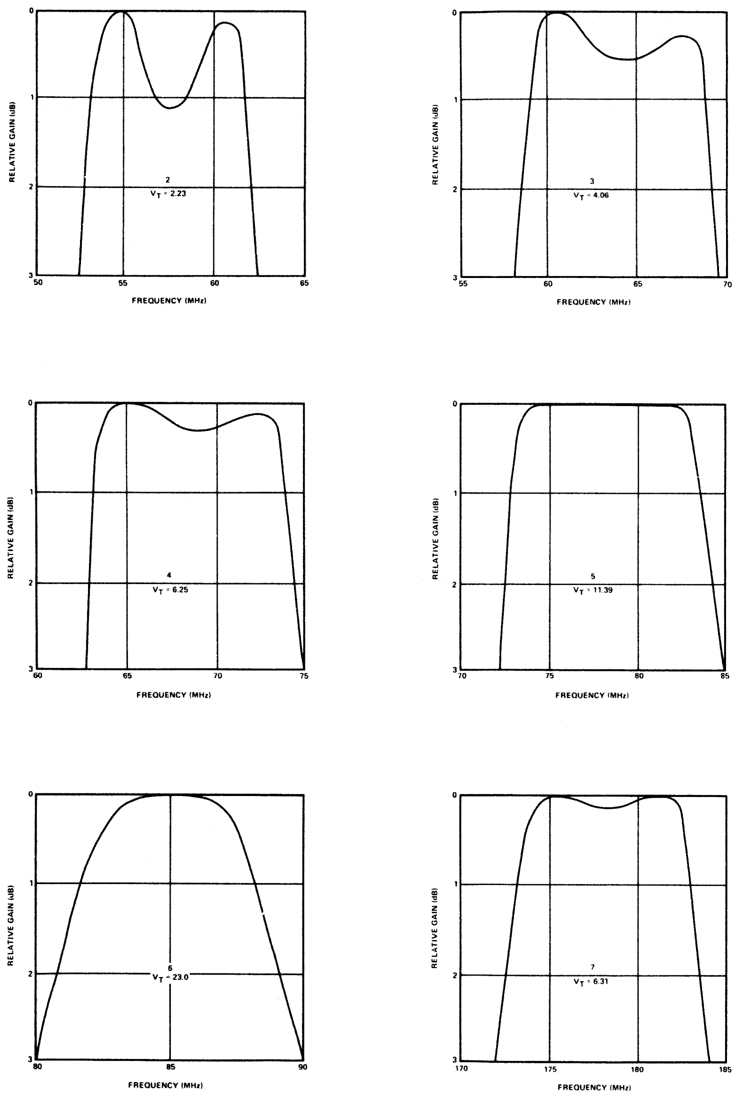
Item	Value	Tolerance
R1	1,500	10%
R2	22,000	20
R3	56,000	5
R4	47,000	20
R5	220,000	5
R6	470	10
R7	47,000	20
R8	47,000	20
R9	115,000	5
R10	3,300	10
R11	10,000	20
R12	27	5
R13	3,300	5
R14	3,300	10
R15	47,000	20
R16	39,000	5
R17	3,300	10
R18	47,000	5
R19	220,000	5
R20	470	5
R21	33,000	5
R22	3,300	10
R23	10,000	5
R24	10,000	10
R25	10,000	5
R26	330	10
R27	1,000	5
R28	680,000	20

NOTE:
R28 is used only with the 75 ohm input model in which case T1 is omitted.

SEMICONDUCTORS

Item	Manufacturer	Part No.
Q1	Signetics	SD306
Q2	Signetics	SD305
Q3	Motorola	MPS HII
D1	Motorola	MPN3401
D2	Motorola	MPN3401
D3	ITT	BB105G
D4	ITT	BB105G
D5	Motorola	MPN3401
D6	Motorola	MPN3401
D7	Motorola	MPN3401
D8	ITT	BB105G
D9	ITT	1N4148
D10	Motorola	MPN3401
D11	ITT	BB105G
D12	ITT	BB105G

RF INTERSTAGE RESPONSE BY CHANNEL

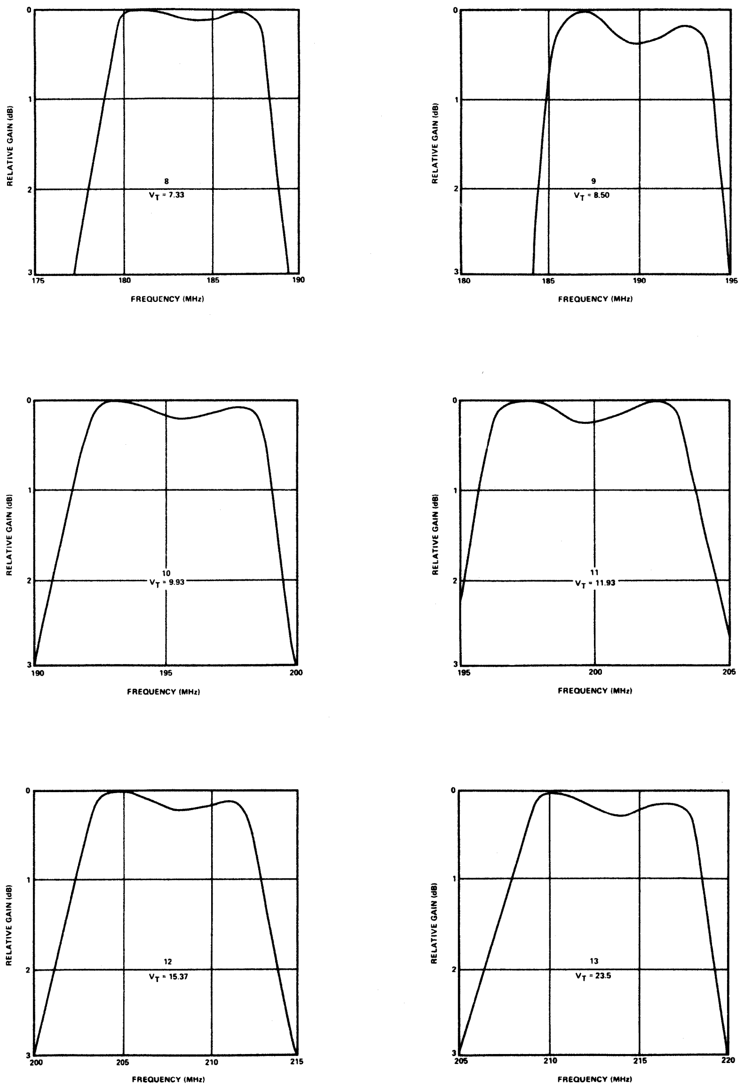


NOTES:

1. Signetics SD306 RF Amplifier and SD305 Mixer.
2. Antenna circuit removed. R_{GEN} = 75Ω.
3. Data taken at Mixer source, drain damped 100Ω local oscillator inactive.
4. Data at maximum gain. Curve remain as shown vs. gain reduction.

FIGURE 2

RF INTERSTAGE RESPONSE BY CHANNEL (Continued)



NOTES:

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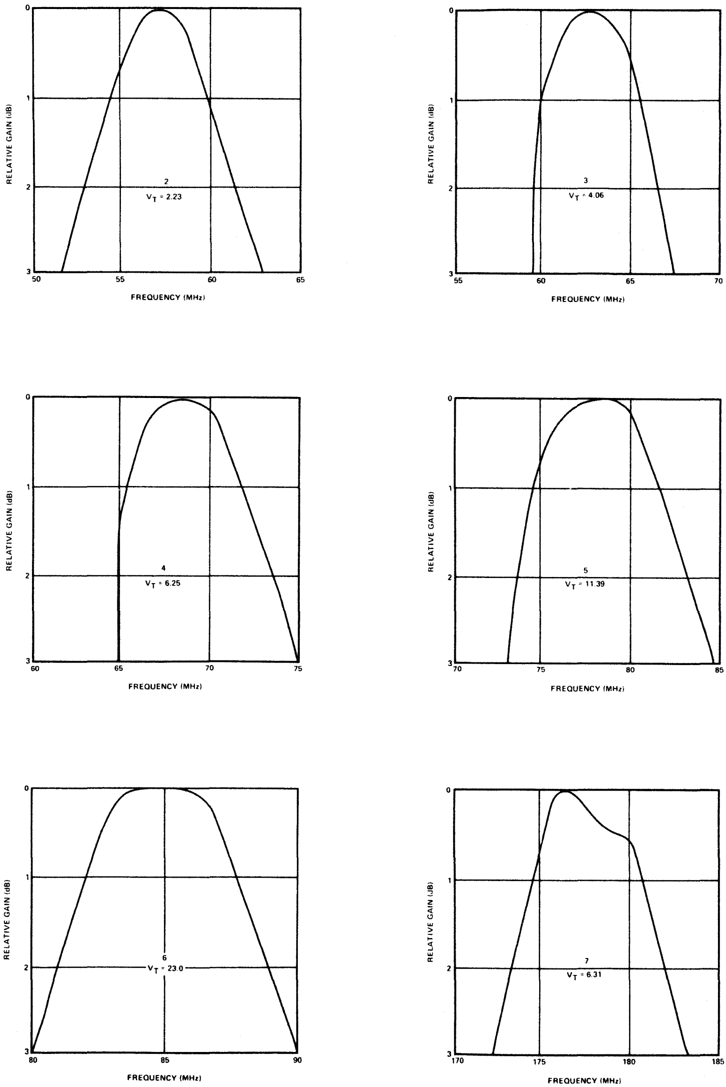
2. Antenna circuit removed. R_{GEN} = 75Ω.
3. Data taken at Mixer source, drain damped 100Ω, local oscillator inactive.
4. Data at maximum gain. Curve remain as shown vs. gain reduction.

FIGURE 2 (Continued)

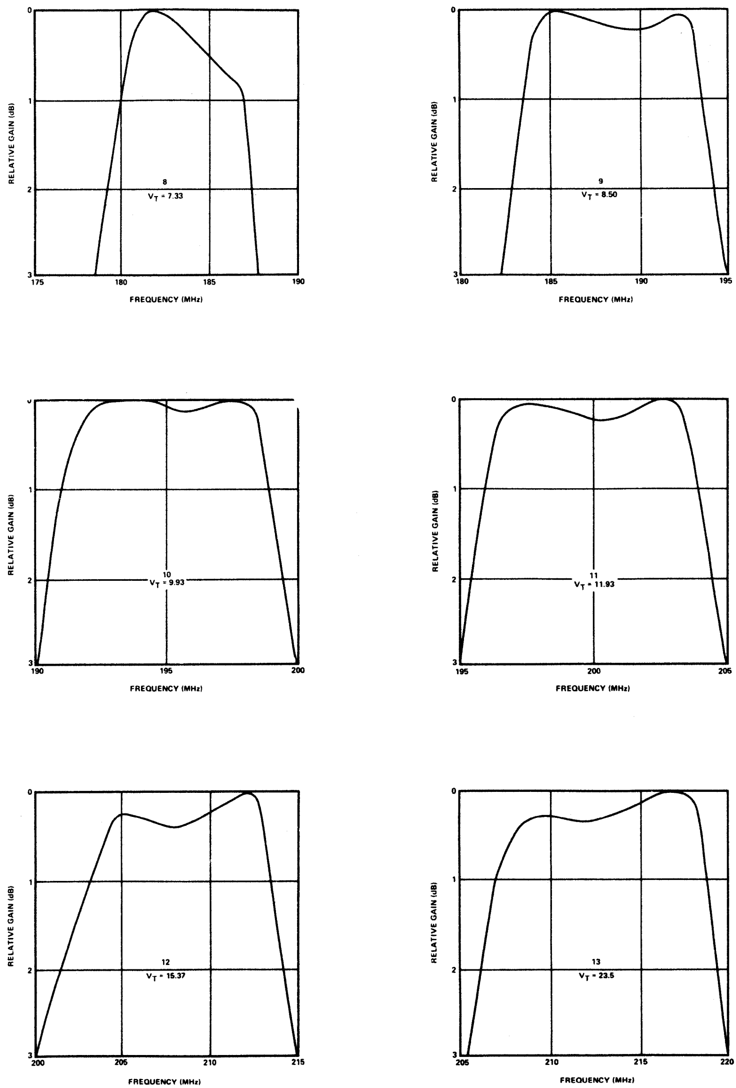
RF RESPONSE BY CHANNEL



NOTES:
1. Signetics SD306 RF Amplifier and SD305 Mixer.
2. Data taken at Mixer source, drain damped 100Ω, local oscillator inactive.
3. Data at maximum gain. Curves for CH2 and 3 become more peaked with gain reduction. Others remain essentially as shown.

FIGURE 3

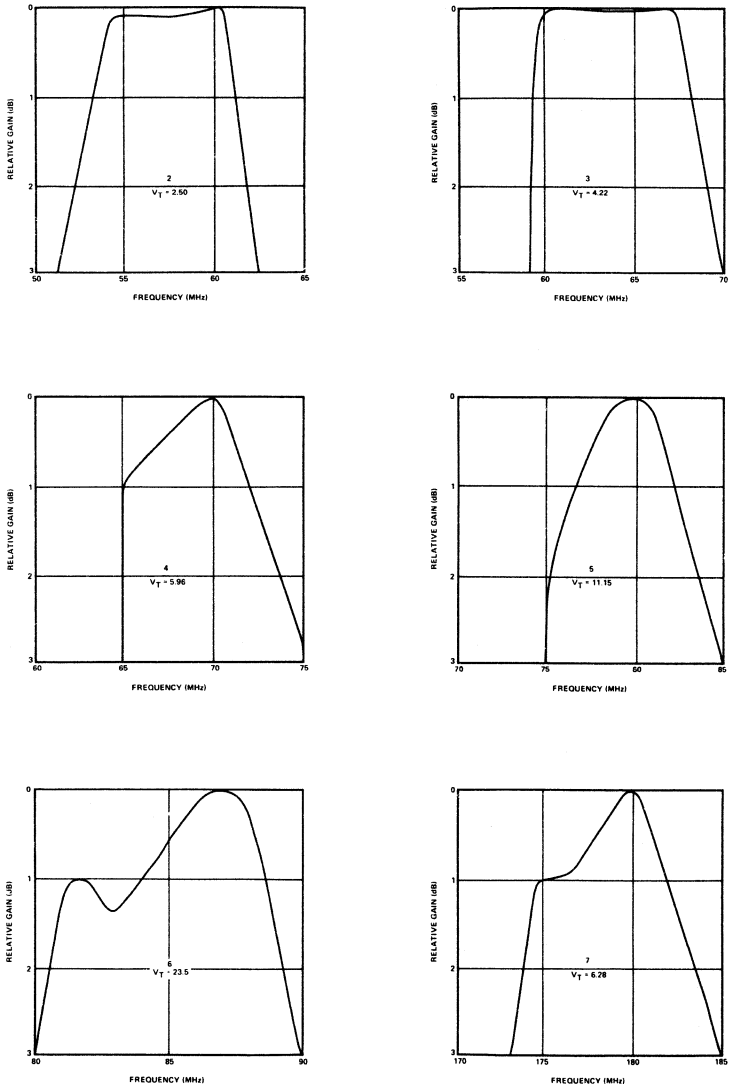
RF RESPONSE BY CHANNEL (Continued)



NOTES:
1. Signetics SD306 RF Amplifier and SD305 Mixer.
2. Data taken at Mixer source, drain damped 100Ω local oscillator inactive.
3. Data at maximum gain. Curves for CH2 and 3 become more peaked with gain reduction. Others remain essentially as shown.

FIGURE 3 (Continued)

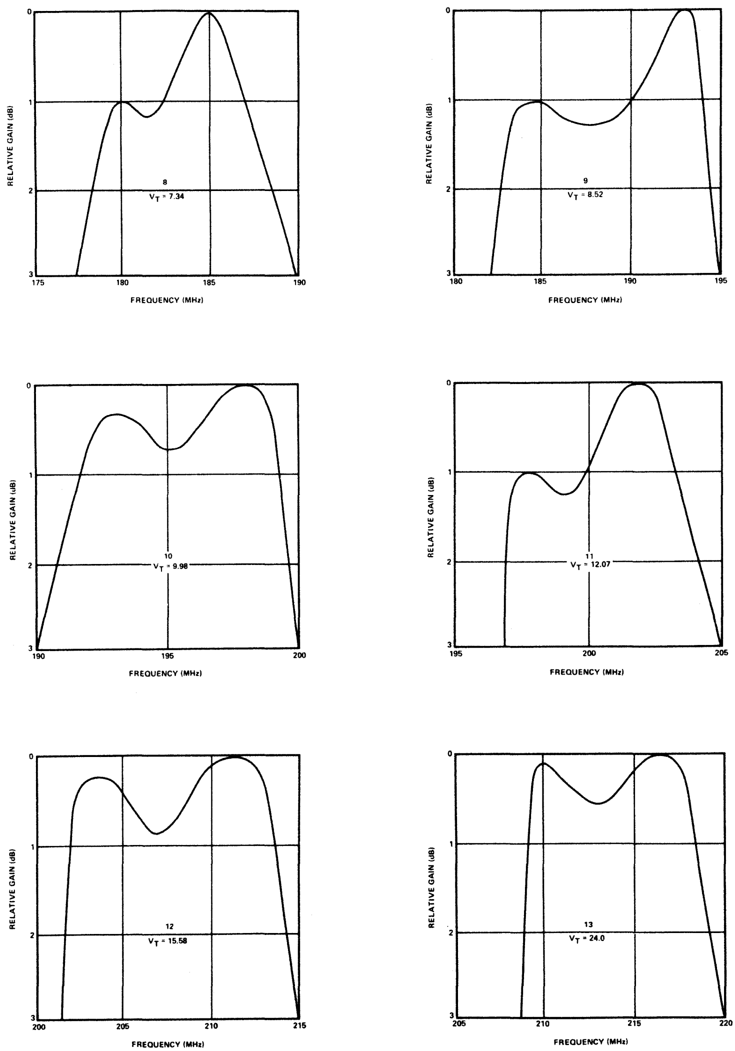
OVERALL RESPONSE BY CHANNEL



NOTES:
1. Signetics SD306 RF Amplifier and SD305 Mixer.
2. Motorola MPS-H11 Oscillator.
3. If center 43.5MHz.
4. Data taken at IF output.
5. Data taken without antenna input filter, $R_{GEN} = 75\Omega$.

FIGURE 4

OVERALL RESPONSE BY CHANNEL (Continued)



NOTES:
1. Signetics SD306 RF Amplifier and SD305 Mixer.
2. Motorola MPS-HII oscillator.
3. IF center 43.5MHz.
4. Data taken at IF output.
5. Data taken without antenna input filter, R_{GEN} = 75Ω.

FIGURE 4 (Continued)

signetics

D-MOS FET QUAD ANALOG SWITCH ARRAYS, MULTIPLEXERS AND DRIVER

ANALOG SWITCHING AND DRIVER APPLICATIONS

SD5000 SD5001 SD5100 SD5101 SD5200

DESCRIPTION

The Signetics D-MOS SD5000, 5100 and 5200 series are monolithic arrays of silicon, insulated-gate, field-effect transistors using the N-channel enhancement mode technology.

This family of devices is designed to handle a wide variety of analog switching and driver applications. They are capable of high speed operation where excellent transient response and wide voltage range are required. The SD5000 quad switch array and the SD5100 quad multiplexer can handle high voltage analog signals (±10V), whereas the SD5001 and SD5101 are designed for lower voltage applications. The SD5200 is intended for use as a 30V driver to complement the other switch products.

FEATURES

- LOW INPUT CAPACITANCE – 2.4pF
- LOW FEEDBACK CAPACITANCE – 0.3pF
- LOW OUTPUT CAPACITANCE – 1.3pF
- ±10V ANALOG SIGNAL RANGE
- LOW PROPAGATION DELAY TIME – 600ps
- LOW ON RESISTANCE – 30Ω
- LOW FEEDTHROUGH AND FEEDBACK TRANSIENTS
- ION IMPLANTED FOR GREATER RELIABILITY
- HIGH CHANNEL-TO-CHANNEL ISOLATION – 107dB
- TRANSIENT PROTECTION FOR GATES

SD5000 APPLICATIONS

ANALOG SWITCHING (UP TO VERY HIGH FREQUENCIES)

AUDIO ROUTING

CHOPPERS

CROSSPOINT SWITCHES

SAMPLE AND HOLD

SD5100 APPLICATIONS

MULTIPLEXING

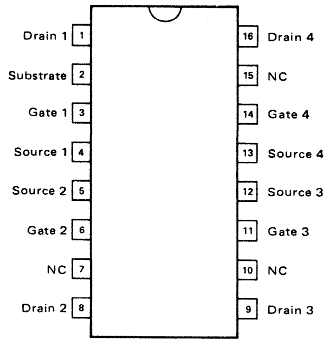
CURRENT SUMMING

SD5200 APPLICATIONS

SWITCH DRIVERS

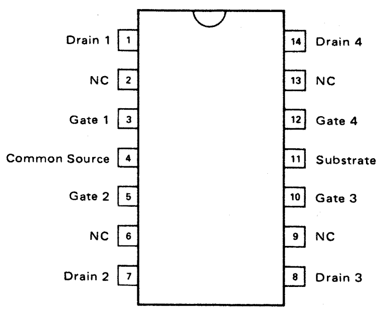
PIN CONFIGURATION (Top View)

B PACKAGE



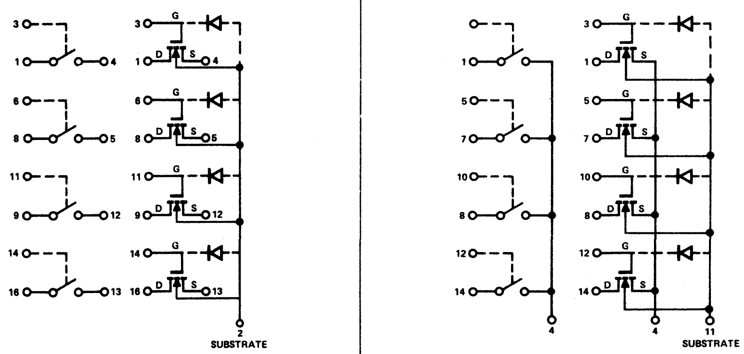
ORDER PART NOS. SD5000B, SD5001B, SD5200B

A PACKAGE



ORDER PART NOS. SD5100A, SD5101A

FUNCTIONAL AND SCHEMATIC DIAGRAMS



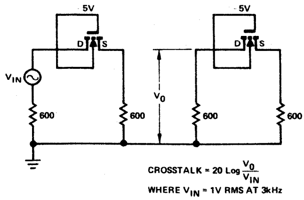
ABSOLUTE MAXIMUM RATINGS T_A = 25°C (Unless Otherwise Noted)

PARAMETER	SD5000	SD5001	SD5100	SD5101	SD5200	UNITS
V_{DS} Drain-To-Source	+20	+10	+30	+15	+30	Vdc
V_{SD} Source-To-Drain	+20	+10	+.5	+.5	+.5	Vdc
V_{DB} Drain-To-Substrate	+25	+15	+30	+15	+30	Vdc
V_{SB} Source-To-Substrate	+25	+15	+.5	+.5	+.5	Vdc
V_{GS} Gate-To-Source	+25 −25	+20 −15	+20	+20	+20	Vdc
V_{GB} Gate-To-Substrate	+30 −0.3	+25 −0.3	+20 −0.3	+20 −0.3	+20 −0.3	Vdc
V_{GD} Gate-To-Drain	+25 −25	+20 −15	+20	+20	+20	Vdc
I_D Drain Current	50	50	50	50	50	mA
Ambient Temperature Range						
Storage Operating	−55 to +150 0 to +85					°C °C
Power Dissipation						
Total Package Dissipation* Individual Transistor Dissipation*	640 300					mW mW

*Derated 5mW per degree centigrade

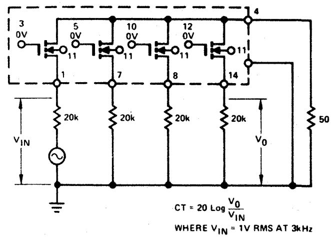
CROSSTALK MEASUREMENT

QUAD SWITCH (SD5000/SD5001)



TEST CIRCUIT NO. 1

MULTIPLEXER (SD5100/SD5101)

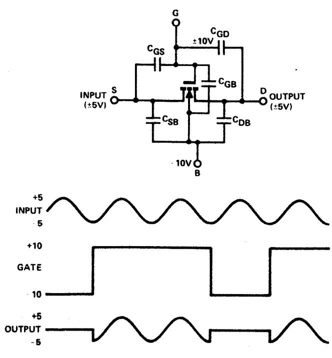


TEST CIRCUIT NO. 2

THEORY OF OPERATION

The SD5000 series consists of four SPST switches with analog signal capability of up to ±10 volts for the SD5000 and up to ±5 volts for the SD5001. Each switch of the array is a D-MOS N-channel field-effect transistor of the enhancement-mode type; that is, the device is normally off when gate-to-source voltage (V_{GS}) is zero volts. When V_{GS} exceeds the threshold voltage V_T the FET switch starts to turn on. With V_{GS} in excess of +10 volts, a low resistance path (typically 30Ω) exists between input and output of the switch. Figure 1 below shows the normal mode of operation of a single switch of the array for ±5 volt analog signal processing. Note that the source is recommended for the input since feedback or reverse transfer capacitance is lower when drain is used as the output. In this case, the switch is driven by ±10 volts for which the SD5200 could be used as discussed later.

FIGURE 1



When analog signals are routed from one point to another the important factors are **isolation, cross-talk** between switches, **feedthrough** and **feedback transients, insertion loss** and **speed** of operation. The SD5000 series offers superior performance in all these areas.

Isolation. ON resistance is typically 30Ω and OFF resistance is typically 10^{10}Ω, which means the OFF to ON resistance ratio is in excess of 10^9. Isolation from output to input from 3kHz analog signals is −107dB.

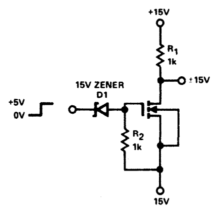
Feedback and feedthrough transients. These are kept to a minimum because of the very low feedback and feedthrough capacitances. This means that "glitchless" or "clean" signals appear at the output.

Insertion loss. This depends upon the source and load impedances involved. As an example for 600Ω source impedance the insertion loss for voice signals (1V RMS at 3kHz) is less than 0.3dB. This indicates that the SD5000 series would make good telephone cross-point switches.

Speed. Because of the low ON resistance and low input capacitance the SD5000 switches turn on at sub-nanosecond speeds. They are also capable of handling very high frequency analog signals and still maintain excellent isolation (20-30dB at 1GHz).

The SD5200 is intended as a driver for the SD5000/5001 but is capable of driving any system which requires ±15 volts. Four drivers are in each package and Figure 2 shows how a single driver is biased for ±15 volts. Two external resistors R_1, R_2 and a zener diode D_1 are required per driver. The input is 5V open collector TTL.

FIGURE 2



The SD5100 series is four channel multiplexers. The SD5100 has 0-30 volts input voltage capability and the SD5101 has 0-15 volts input voltage capability. Each circuit has a common source. The signals at the source are limited to ±200mV and therefore these circuits are used where switching is performed at the virtual ground point of an op amp. In this case, no external driver is required nor are any additional power supplies required. Because the ON resistance of both the SD5000 and SD5001 is very low (30Ω typ) and matched within 5Ω, the need for a compensating FET is minimized and in some cases eliminated. The parts can be driven directly from TTL, either +5 volts or +15 volts open collector.

ANALOG SWITCH/DRIVER APPLICATION

The SD5200 operates as an inverting switch capable of driving 30 volts maximum. This wide range capability with high speed fulfills most analog switching applications. Figure 3 demonstrates how the SD5200 drives the SD5000 in a typical analog switching application.

ANALOG MULTIPLEXER APPLICATION

The SD5100 series is easy to use as shown in Figure 4. Drive circuitry can be TTL or if very low R_{ON} is required (19Ω typ), then TTL open collector logic can drive the SD5100 up to +20 volts. The common source is kept at or near

FIGURE 3

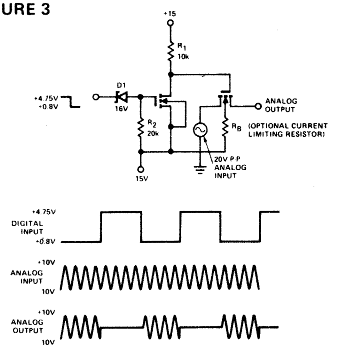
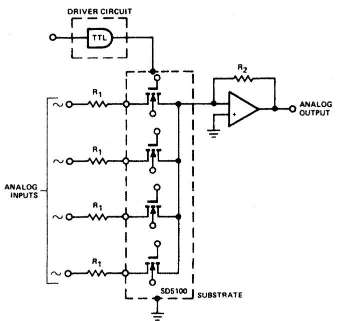


FIGURE 4



ELECTRICAL CHARACTERISTICS $T_A = +25°C$

PARAMETER	
Breakdown Voltage	
BV_{DS}	Drain-To-Source
BV_{SD}	Source-To-Drain
BV_{DB}	Drain-To-Substrate
BV_{SB}	Source-To-Substrate
Leakage Current	
I_{DS} (OFF)	Drain-To-Source
I_{SD} (OFF)	Source-To-Drain
I_{GBS}	Gate
I_{GB}	Gate-To-Substrate
V_T	**Threshold Voltage**
gfs	**Forward Transconductance**
Small Signal Capacitances	
$C_{(GS + GD + GB)}$	Gate Node
$C_{(GD + DB)}$	Drain Node
$C_{(GS + SB)}$	Source Node
C_{DG}	Reverse Transfer
C_T	**Cross Talk**
r_{DS} (ON)	**Drain-To-Source Resistance**
r_{DSM} (ON)	**Resistance Match**

ground and each drain will withstand +30 volts with isolation typically 120dB.

If a compensation transistor is required in series with R_2, then the maximum mismatch error for $R_1 = R_2 = 10k\Omega$ would be:

TEST CONDITIONS	SD5000			SD5001			SD5100			SD5101			SD5200			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{GS} = V_{BS} = -5V$, $I_S = 10nA$	20	25		10	25											V
$V_{GS} = V_{BS} = 0V$, $I_S = 1\mu A$							30	35		15	30					V
$V_{GS} = V_{BS} = 0V$, $I_S = 10\mu A$													30	35		V
$V_{GD} = V_{BD} = -5V$, $I_D = 10nA$	20			10												V
$V_{GD} = V_{BD} = 0V$, $I_D = 10nA$							.5			.5						V
$V_{GB} = 0V$, Source OPEN																
$I_D = 10nA$	25			15												V
$I_D = 1\mu A$							30			15						V
$V_{GB} = 0V$, Drain OPEN																
$I_S = 10\mu A$	25			15												V
$I_S = 100nA$							.5			.5						V
$V_{GS} = V_{BS} = -5V$																
$V_{DS} = +20V$		1	10													nA
$V_{DS} = +10V$					1	10										nA
$V_{GS} = V_{BS} = 0V$, $V_{DS} = +10V$								1	10		1	10				nA
$V_{GD} = V_{BD} = -5V$																
$V_{SD} = +20V$		1	10													nA
$V_{SD} = +10V$					1	10										nA
$V_{DB} = V_{SB} = 0V$																
$V_{GB} = 25V$			10													µA
$V_{GB} = 20V$						10			10			10			10	µA
Drain and Source OPEN																
$V_{GB} = +30V$			1													µA
$V_{GB} = +25V$						1										µA
$V_{DS} = V_{GS} = V_T$, $I_S = 1\mu A$, $V_{SB} = 0V$	0.1	1.0	2.0	0.1	1.0	2.0	0.5	1.0	2.0	0.5	1.0	2.0	0.5	1.0	2.0	V
$V_{DS} = 10V$, $V_{SB} = 0V$, $I_D = 20mA$, f = 1kHz	10	15		10	15		10	15		10	15		10	15		mmhos
$V_{DS} = 10V$, f = 1MHz, $V_{GS} = V_{BS} = -15V$																
See Capacitance Model in Figure 1		2.4	3.5		2.4	3.5		2.4	3.5		2.4	3.5		2.4	3.5	pF
		1.3	1.5		1.3	1.5		1.3	1.5		1.3	1.5		1.3	1.5	pF
		3.5	4.0		3.5	4.0										pF
		0.3	0.5		0.3	0.5		0.3	0.5		0.3	0.5		0.3	0.5	pF
See Test Circuits No. 1 & 2, f = 3kHz								-107								dB
$I_D = 0.1mA$, $V_{SB} = 0$																
$V_{GS} = +5V$								50	70							Ω
$V_{GS} = +10V$								30	45							Ω
$V_{GS} = +15V$								23								Ω
$V_{GS} = +20V$								19								Ω
$I_D = 0.1mA$, $V_{SB} = 0$, $V_{GS} = +5V$								1	5					—		Ω

$$\text{error} = \frac{R_2 + 65\Omega}{R_1 + 70\Omega} = .05\%$$

Without the compensation transistor the error would be:

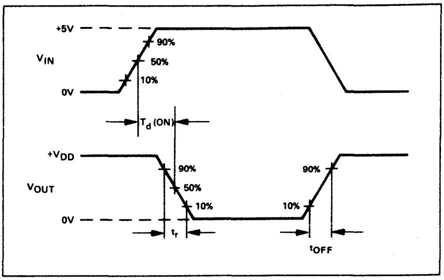
$$\text{error} = \frac{R_2}{R_1 + 70\Omega} = .7\%$$

SWITCHING CHARACTERISTICS

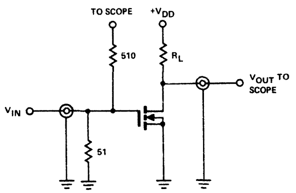
		t_d (ON) (ns)		t_r (ns)		t_{OFF} (ns)	
V_{DD}	R_L	TYP	MAX	TYP	MAX	TYP	MAX
5	680	0.6	1.0	0.7	1.0	9.0	*
10	680	0.7		0.8		9.0	
15	1k	0.9		1.0		14.0	

*t_{OFF} is dependent on R_L and C_L and does not depend on the device characteristics.

SWITCHING WAVEFORMS



TEST CIRCUIT



INPUT PULSE

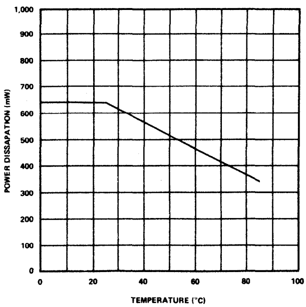
t_r, t_f < 1ns
PULSE WIDTH = 100 ns
REP RATE = 1 MHz

SAMPLING SCOPE

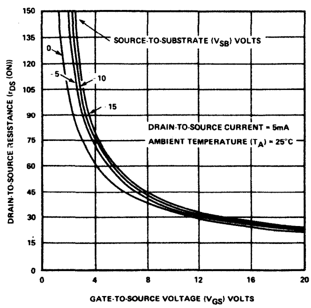
t_r < 350 ps
R_{IN} = 1 MΩ
C_{IN} = 2.0 pF

CHARACTERISTIC CURVES

MAXIMUM POWER DISSIPATION VS TEMPERATURE

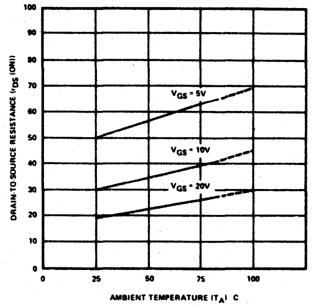


DRAIN-TO-SOURCE RESISTANCE VS SOURCE-TO-SUBSTRATE AND GATE-TO-SOURCE VOLTAGE

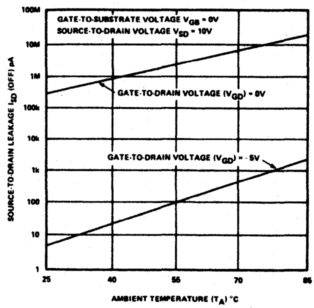


CHARACTERISTIC CURVES (Continued)

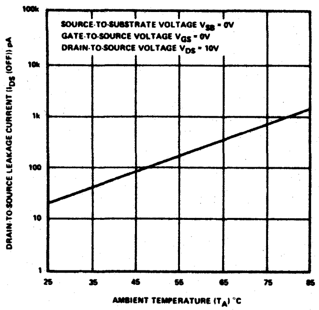
DRAIN-TO-SOURCE RESISTANCE VS TEMPERATURE



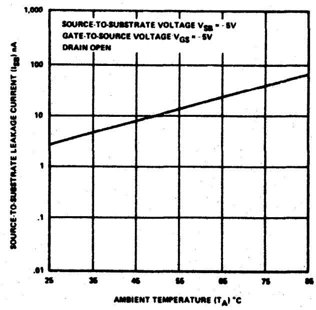
SOURCE-TO-DRAIN LEAKAGE CURRENT VS TEMPERATURE



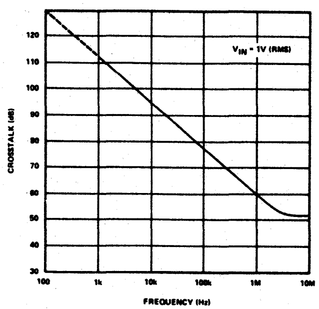
DRAIN-TO-SOURCE LEAKAGE CURRENT VS TEMPERATURE



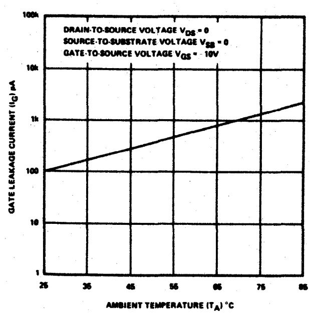
SOURCE-TO-SUBSTRATE LEAKAGE CURRENT VS TEMPERATURE



CROSSTALK VS FREQUENCY



GATE LEAKAGE CURRENT VS TEMPERATURE



signetics

D-MOS DUAL-GATE FETs N-CHANNEL ENHANCEMENT | SD6000

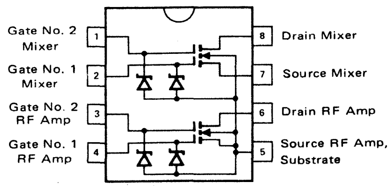
FM AND VHF FRONT-END APPLICATIONS

DESCRIPTION

The Signetics D-MOS SD6000 is an integrated circuit fabricated by the double-diffused process and employing silicon N-channel enhancement mode MOSFETs with dual gates. Zener diodes are connected between all gates and the substrate. These diodes bypass any voltage transients which lie outside the range of −0.3V to +20.0V. Thus, the gates are protected against damage in all normal handling and operating situations. The use of the dual gate structure plus the incorporation of the drift region has made the feedback capacity (C_{G1D}) typically less than 0.03pF. The attributes of the IC make it ideally suited for FM/VHF RF amplifier and mixer applications. The IC is specifically characterized for incorporation into varactor or conventional FM tuners but the performance guaranteed makes it useful in a wide variety of VHF tuner applications. The power gain at 100MHz is 30dB minimum with a guaranteed noise figure of 3.0dB. A wide AGC capability plus significant reduction in cross modulation is now available because of the inherent linearity of the D-MOS FETs. The SD6000 is packaged in the Signetics 8-pin plastic V package.

PIN CONFIGURATION (Top View)

V PACKAGE



ORDER PART NO. SD6000V

GENERAL FEATURES

- POSITIVE BIAS ONLY
- LOW GATE VOLTAGES
- ENHANCEMENT MODE OPERATION
- ZENER DIODE GATE PROTECTION
- ION IMPLANTED FOR GREATER RELIABILITY

FEATURES (RF AMP Section)

- HIGH POWER GAIN WITHOUT NEUTRALIZATION – 25dB AT 100MHz
- LOW NOISE FIGURE – 2.5dB AT 100MHz
- LOW INPUT AND OUTPUT CAPACITANCES CONSTANT WITH AGC – 3.0pF AND 1.0pF
- LOW FEEDBACK CAPACITANCE – 0.025pF
- SUPERIOR CROSS MODULATION PERFORMANCE
- HIGH TRANSCONDUCTANCE – 15mmhos
- WIDE AGC RANGE – 50dB AT 100MHz

FEATURES (Mixer Section)

- HIGH CONVERSION GAIN – 17dB AT 100MHz WITH V_{G1S} = V_{G2S} FOR BIASING SIMPLICITY
- EXCELLENT ISOLATION FROM GATE NO. 1 (RF) TO GATE NO. 2 (LO)
- LOW INPUT CAPACITANCE – 4.0pF
- LOW FEEDBACK CAPACITANCE – 0.03pF
- EXCELLENT CROSS MODULATION PERFORMANCE AND LOW NOISE OPERATION
- HIGH CONVERSION TRANSCONDUCTANCE AT LOW DRAIN CURRENTS – 10mmhos

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C (Unless Otherwise Noted)

V_{DS}	Drain-To-Source Voltage	+20V
V_{G1B}	Gate No. 1-To-Substrate Voltage	−0.3 to +20Vdc
V_{G2B}	Gate No. 2-To-Substrate Voltage	−0.3 to +20Vdc
	Drain Current	50mA
T_A	Ambient Temperature Range	
	Storage	−65°C to +150°C
	Operating	−65°C to +125°C
P_T	Power Dissipation	
	At 25°C Case Temperature	625mW
	Temperature Above 25°C	Derate at 5.0mW/°C

ELECTRICAL CHARACTERISTICS $T_A = 25°C$

PARAMETER		TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
OFF Characteristics — RF Amp and Mixer						
BV_{DS}	Drain-To-Source Breakdown Voltage	$V_{G1S} = V_{G2S} = 0V$, $I_D = 5\mu A$	20	30		V
$I_{D(OFF)}$	Drain-To-Source Leakage Current	$V_{DS} = +15V$, $V_{G1S} = V_{G2S} = 0V$		0.001	1.0	μA
$I_{D\,SS}$	Zero Bias Drain Current	$V_{DS} = +15V$, $V_{G1S} = V_{G2S} = 0V$		0.001	1.0	μA
I_{G1SS}	Gate No. 1 Leakage Current	$V_{G1S} = +5V$, $V_{G2S} = V_{DS} = 0V$		0.001	0.1	μA
I_{G2SS}	Gate No. 2 Leakage Current	$V_{G2S} = +10V$, $V_{G1S} = V_{DS} = 0V$		0.001	0.1	μA

ON Characteristics			RF AMP MIN	RF AMP TYP	RF AMP MAX	MIXER MIN	MIXER TYP	MIXER MAX	
V_{T1}	Gate 1 Threshold Voltage	$V_{DS} = V_{G1S} = V_{T1}$, $V_{G2S} = +10V$, $I_D = 1\mu A$	0.1	0.5	1.5	0.1	1.0	2.0	V
V_{T2}	Gate 2 Threshold Voltage	$V_{DS} = V_{G2S} = V_{T2}$, $V_{G1S} = +5V$, $I_D = 1\mu A$	0.1	0.5	1.5	0.1	1.0	2.0	V
$r_{DS(ON)}$	Drain-To-Source On Resistance	$V_{G1S} = +5V$, $V_{G2S} = +10V$, $I_D = 0.1mA$		65	100		30	60	Ω

Small Signal Characteristics — RF Amp			MIN	TYP	MAX	
gfs	Forward Transconductance	$V_{DS} = +15V$, $V_{G2S} = +10V$, $I_D = 18mA$, f = 1kHz	12	15		mmhos
Capacitances		f = 1MHz, Gate No. 2 AC Grounded				
C_{G1S}	Input	$V_{DS} = +15V$, $V_{G2S} = +10V$, $I_D = 18mA$		3.0	3.5	pF
C_{DS}	Output	$V_{DS} = +15V$, $V_{G1S} = 0V$, $V_{G2S} = 10V$		1.0	1.3	pF
C_{G1D}	Reverse Transfer	$V_{DS} = +15V$, $V_{G1S} = 0V$, $V_{G2S} = 10V$		0.025		pF
Input Admittance		f = 100MHz, $V_{DS} = +15V$, $V_{G2S} = +10V$, $I_D = 18mA$				mmhos
Re (y_{11})				0.21		
Im (y_{11})				2.26		
Output Admittance						
Re (y_{22})				0.20		
Im (y_{22})				0.68		
Forward Transmittance						
Re (y_{21})				12.85		
Im (y_{21})				−1.50		
Reverse Transmittance						
Re (y_{12})				0.01		
Im (y_{12})				−0.03		
Gps	Power Gain*	$V_{DS} = +15V$, $V_{G2S} = +10V$, $I_D = 18mA$, f = 100MHz	20	25		dB
NF	Noise Figure*	$V_{DS} = +15V$, $V_{G2S} = +10V$, $I_D = 18mA$, f = 100MHz		2.5	3.0	dB
AGC(V_{G2S})	Range Of Automatic Gain Control	$V_{DS} = +15V$, $V_{G1S} \cong +2.5V$, f = 100MHz		50		dB

ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$

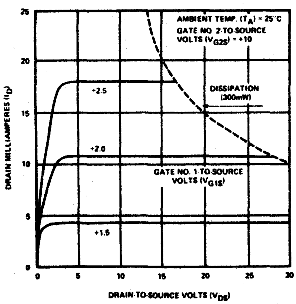
PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Small Signal Characteristics – MIXER					
$gfs_{(CONV)}$ Conversion Transconductance	$V_{DS} = +15V$, $V_{G1S} = V_{G2S}$ $I_D = 8mA$, $f = 1kHz$ E_{LO} (RMS) = 750mV		10		mmhos
Capacitances	f = 1MHz, Gate No. 2 AC Grounded				
C_{GIS} Input	$V_{DS} = +15V$, $V_{G1S} = V_{G2S}$, $I_D = 8mA$		4.0	4.75	pF
C_{DS} Output	$V_{DS} = +15V$, $V_{G1S} = V_{G2S} = 0V$		1.1	1.5	pF
C_{G1D} Reverse Transfer	$V_{DS} = +15V$, $V_{G1S} = V_{G2S} = 0V$		0.030		pF
Input Admittance	f = 100MHz, $V_{DS} = +15V$ $V_{G1S} = V_{G2S}$, $I_D = 8mA$				
Re (y_{11})			0.21		
Im (y_{11})			2.28		
Output Admittance					
Re (y_{22})			0.41		
Im (y_{22})			1.04		
Forward Transmittance					
Re (y_{21})			3.18		
Im (y_{21})			−0.83		
Reverse Transmittance					
Re (y_{12})			0.03		
Im (y_{12})			−0.01		
$Gps_{(CONV)}$ Conversion Power Gain**	$V_{DS} = +15V$, $V_{G1S} = V_{G2S}$, $I_D = 8mA$, $f_{RF} = 100MHz$, $f_{LO} = 89.3MHz$	14	19		dB

*Measured in Amplifier test fixture.
**Measured in MIXER test fixture.

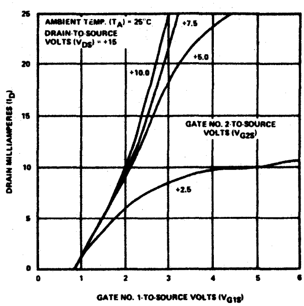
CHARACTERISTIC CURVES

RF AMP SECTION

DRAIN CURRENT VS DRAIN-TO-SOURCE VOLTAGE



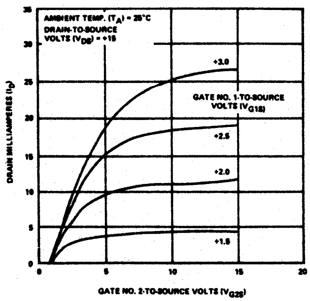
DRAIN CURRENT VS GATE NO. 1-TO-SOURCE VOLTAGE



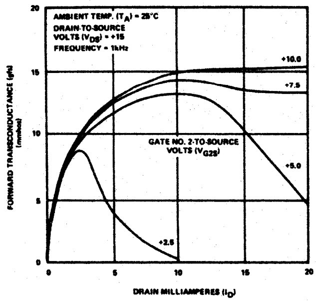
CHARACTERISTIC CURVES (Continued)

RF AMP SECTION

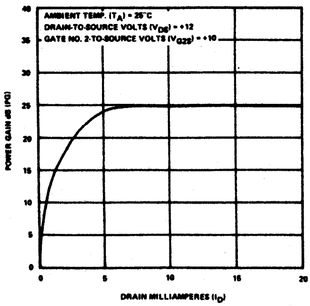
DRAIN CURRENT VS GATE NO. 2-TO-SOURCE VOLTAGE



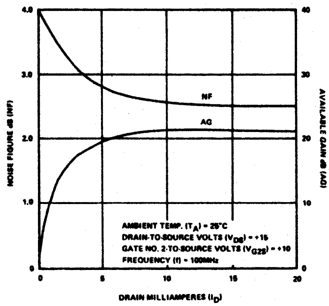
1kHz FORWARD TRANSCONDUCTANCE VS DRAIN CURRENT



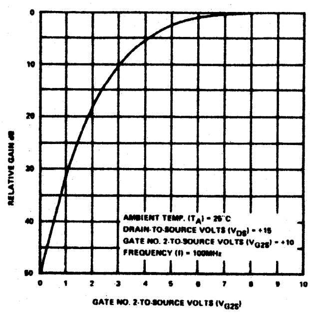
POWER GAIN VS DRAIN CURRENT



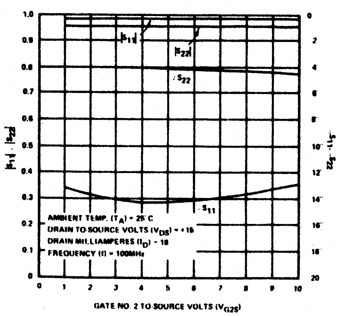
NOISE FIGURE AND AVAILABLE GAIN VS DRAIN CURRENT



AUTOMATIC GAIN CONTROL RANGE



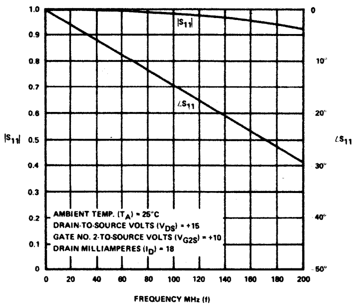
S_{11} AND S_{22} VS GATE NO. 2-TO-SOURCE VOLTAGE



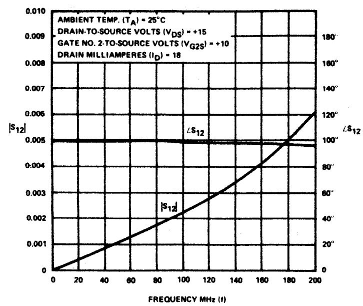
CHARACTERISTIC CURVES (Continued)

RF AMP SECTION

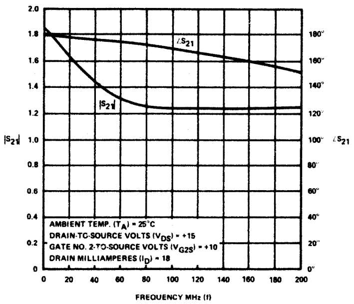
S_{11} VS FREQUENCY



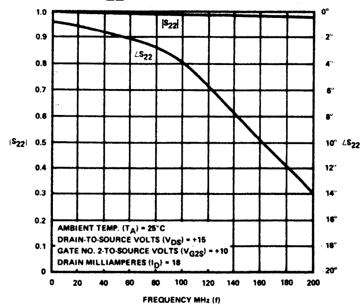
S_{12} VS FREQUENCY



S_{21} VS FREQUENCY

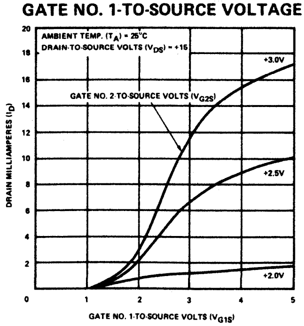


S_{22} VS FREQUENCY

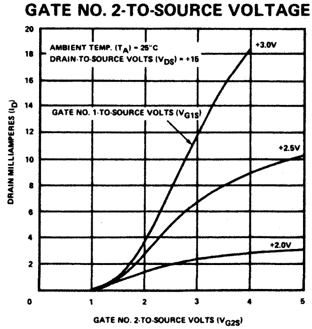


MIXER SECTION

DRAIN CURRENT VS GATE NO. 1-TO-SOURCE VOLTAGE



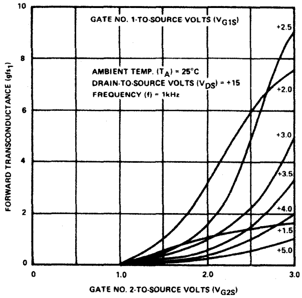
DRAIN CURRENT VS GATE NO. 2-TO-SOURCE VOLTAGE



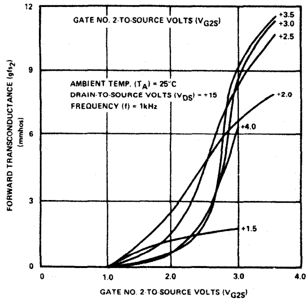
CHARACTERISTIC CURVES (Continued)

MIXER SECTION

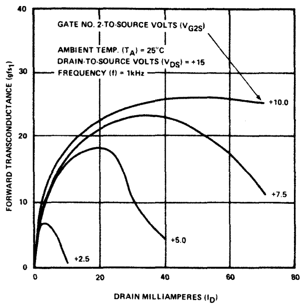
GATE NO. 1 FORWARD TRANSCONDUCTANCE VS GATE NO. 2-TO-SOURCE VOLTAGE



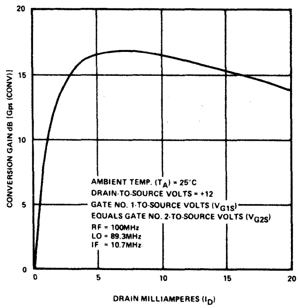
GATE NO. 2 FORWARD TRANSCONDUCTANCE VS GATE NO. 1-TO-SOURCE VOLTAGE



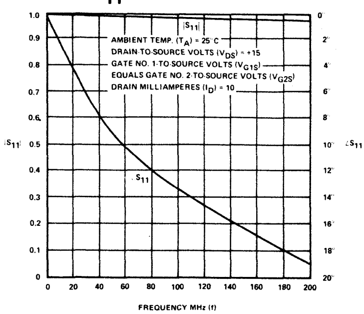
GATE NO. 1 FORWARD TRANSCONDUCTANCE VS DRAIN CURRENT



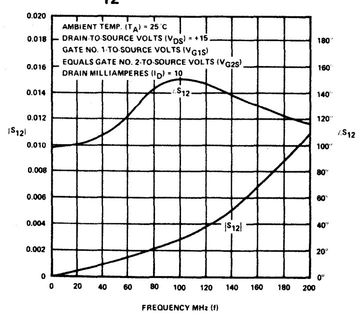
CONVERSION GAIN VS. DRAIN CURRENT



S_{11} VS FREQUENCY



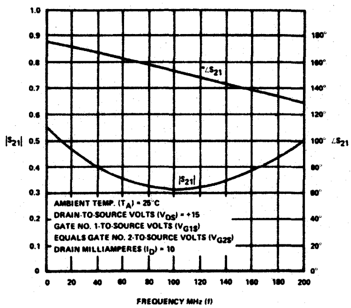
S_{12} VS FREQUENCY



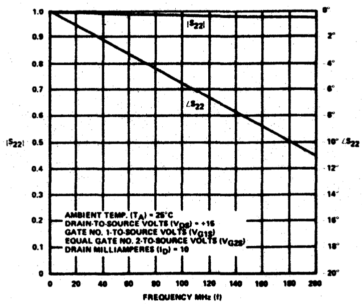
CHARACTERISTIC CURVES (Continued)

MIXER SECTION

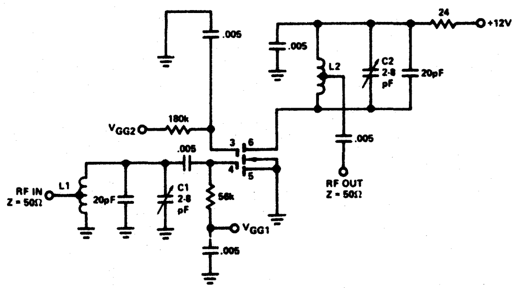
S_{21} VS FREQUENCY



S_{22} VS FREQUENCY

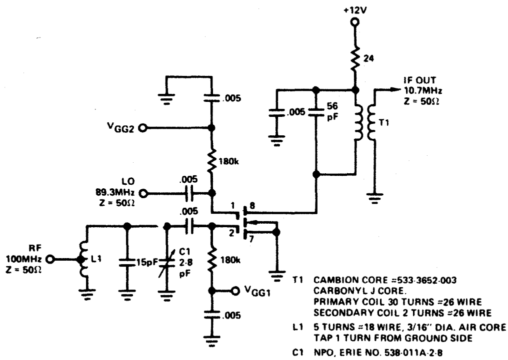


RF AMP SECTION TEST CIRCUIT



L1-L2 5 TURN #18 WIRE 3/16" DIA. AIR CORE TAPPED AT 1 TURN
C1-C2 NPO, ERIE NO. 538-011A-2-8

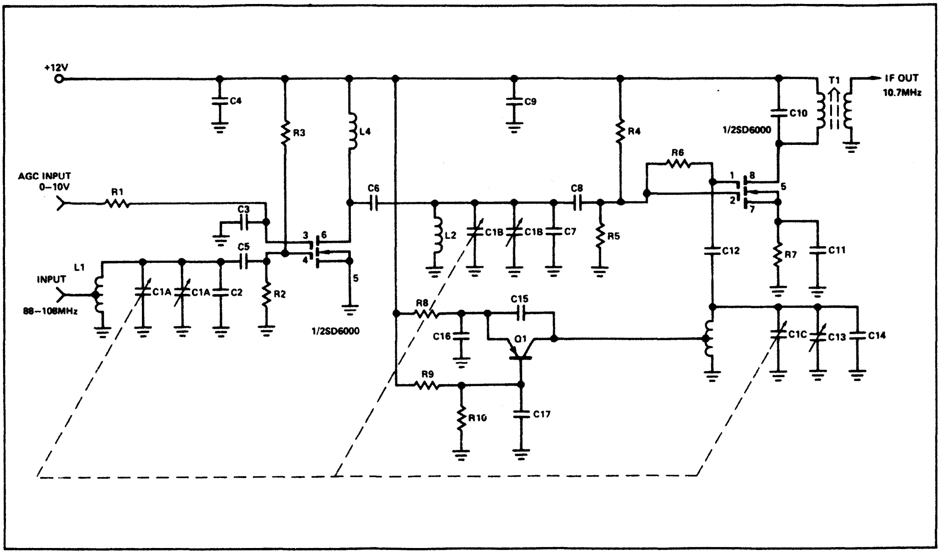
MIXER SECTION TEST CIRCUIT



FM TUNER USING SD6000 ELECTRICAL DATA

PARAMETER	TEST CONDITIONS	TYP
Supply Voltage		+12V
Supply Current	AGC voltage +10V	25mA
Frequency Range		88MHz to 108MHz
Bandwidth	RF Amp (−3dB) Mixer (−3dB)	2.5MHz 300kHz
Input Impedance		75Ω
Output Impedance		50Ω
IF Output Frequency		10.7MHz
Oscillator Stability w/respect to Supply Voltage		40kHz/volt
Oscillator Stability w/respect to Temperature		10kHz/°C
Power Gain	88MHz to 108MHz	30dB Min
Noise Figure	@ 100MHz	3.0dB Max

FM TUNER USING SD6000



PARTS LIST

1. Transistors

	Description	**Type**
Q1	PNP Silicon	2N4126

2. Integrated Circuits

U1	Dual D-MOS FET	SD6000V

3. Resistors (All carbon resistors in ohms ±10% tolerance.)

	Value
R1	30k
R2	68k
R3	200k
R4	150k
R5	39k
R6	82k
R7	120
R8	6800
R9	13k
R10	3k

4. Capacitors

	Value	**Type**
C1	5-20pF	3 Gang Tuning Capacitor
C2	20pF	±5% NPO
C3, 4, 5, 6, 8, 9, 11, 12, 17	.005	+80% – 20% Ceramic
C7	10pF	±5% NPO
C10	56pF	±5% MICA or Ceramic
C13	2-8pF	Trimmer
C14	12pF	±5% NPO
C15	10pF	±5% NPO
C16	10pF	±5% NPO

5. Miscellaneous Components

T1	IF Transformer	Cambion 533-3652-003 Jcore Prim. 30T #26 Sec. 2T #26
L1	RF Input Coil	4 turns #18 on 3/16" dia. Air core – Tap 1 turn from ground side.
L2	RF Output Coil	4 turns #18 on 3/16" dia. air core.
L3	Oscillator Coil	4 turns #18 on 3/16" dia. air core center-tapped.
L4		33μh RF choke

signetics

APPLICATIONS MEMO SD6000

LINEAR DEVICES
FM TUNER

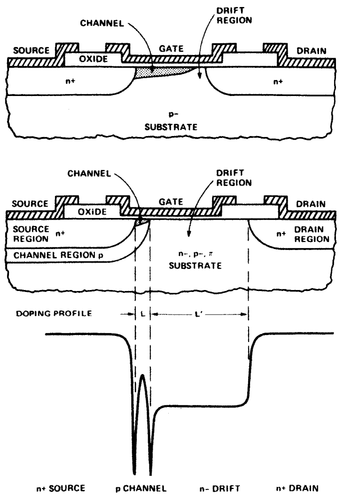
INTRODUCTION

Signetics dual D-MOS FETs are dual gate n-channel enhancement mode MOSFETs fabricated by a new state-of-the-art technique. They make it possible for the tuner designer to obtain the high performance typical of D-MOS at a cost competitive with bipolars. Dual gate D-MOS has inherently linear characteristics making it especially suitable in FM tuner RF stages where high RF and conversion gain, low noise figure, wide dynamic range, and excellent cross-modulation and intermodulation characteristics are necessary.

CONSTRUCTION

An understanding of the basic differences in the construction of Signetics D-MOS vs. the conventional MOSFET is very helpful in realizing the maximum benefits of D-MOS.

Construction of D-MOS transistors is basically different from a conventional n-channel MOSFET in that it contains a lowly doped region of length L' between the channel p region and the highly n doped drain contact region, as shown in Figure 1. Generally, MOS transistor frequency response is directly related to channel length (L) and parasitic capacitances, improving as they decrease.



DOPING PROFILE ACROSS D-MOS TRANSISTOR (BOTTOM) DIFFERS FROM CONVENTIONAL MOS DEVICE: PROFILE IS NONUNIFORM IN THE NARROW CHANNEL REGION. MOST OF THE CONDUCTANCE-MODULATION TAKES PLACE IN THE CHANNEL, WHICH HAS CHARACTERISTICS THAT CONTROL THE DEVICE'S SPEED AND GAIN.

FIGURE 1
DOPING PROFILE

D-MOS construction permits a precisely controlled L of less than 1 micron, extremely low parasitic capacitances and additionally, no restriction on maximum drain breakdown voltage. Although the construction differs, operation of D-MOS is similar to that of ordinary MOSFETs. Positive voltage applied between gate and source controls the number of carriers in the channel, and therefore, the conductivity.

FM TUNER DESIGN

The purpose of this design was to build an FM tuner using dual gate D-MOS FETs, in an economical epoxy package, to verify their superior performance. Careful consideration was given to the problems involved in putting two devices in the same package. The die were placed in the package in a manner that minimizes the coupling from one device to the other. This was done to keep the L.O. isolated from the RF input and for stability.

The AC performance characteristics of the SD6000 given on the data sheet are used for this design. The input and output matching networks are designed using scattering parameters.

This data is given below in Figure 2.

	Frequency (MHz)	S_{11}	S_{12} (dB)	S_{21} (dB)	S_{22}
RF Amp	100	$.98\angle -14$	$-50\angle 80$	$3\angle 165$	$.98\angle -6$
Mixer	100	$.98\angle -18$	$-47\angle 90$	$-5.2\angle 150$	$.96\angle -6$

FIGURE 2
SD6000 S-PARAMETERS

The s-parameters given in Figure 2 can be readily converted to y-parameters. The RF amplifier can then be designed using classical "two port network" theory. A problem exists, however, when the s-parameters (S_{11} and S_{22}) magnitudes are very close to unity. When this is the case, a small change in magnitude of S_{11} or S_{22} gives a large change in Y_{11} and Y_{22}. For example, the s-parameters given for the RF amplifier device in Figure 2 give

$$Y_{11} = .2 + j\ 2.43\ \text{(mmhos)}$$
$$Y_{22} = .2 + 1.03\ \text{(mmhos)}$$

If S_{11} and S_{22} are equal to .99 instead of .98 we get

$$Y_{11} = .1 + j\ 2.43\ \text{(mmhos)}$$
$$Y_{22} = .1 + j\ 1.03\ \text{(mmhos)}$$

This means that a 1% error in measuring S_{11} or S_{22} will give a 2 to 1 change in the real part of the devices' input or output impedance. This makes a paper design questionable unless some assumptions are made. For this tuner design the device input and output equivalent circuits were approximated as shown in Figure 3:

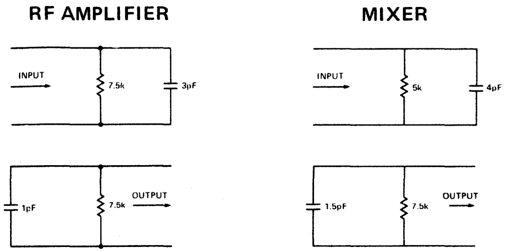


FIGURE 3
INPUT AND OUTPUT EQUIVALENT CIRCUITS

These approximations make the design much easier and were verified by the final tuner performance.

INPUT CIRCUIT

The high input impedance of the SD6000 makes it possible to have a high Q input circuit. This makes the tuner very selective and free from spurious responses. Figure 4 shows the equivalent input circuit.

A 70 nh inductor was chosen to allow the tuner to cover the FM band with a ΔC of $\approx$ 18pF. The required capacitance ratio can be found in the following way:

$\omega_1 = 2\pi f_1$ $\quad\omega_1$ = radian frequency at the low end of the FM band.

$\omega_2 = 2\pi f_2$ $\quad\omega_2$ = radian frequency at the high end of the FM band.

$\omega_1{}^2 = \frac{1}{LC_1}$ $\quad C_1$ = required capacitance at low frequency.

$\omega_2{}^2 = \frac{1}{LC_2}$ $\quad C_2$ = required capacitance at high end.

Therefore $\omega_1{}^2\, C_1 = \omega_2{}^2\, C_2$

or $\frac{C_1}{C_2} = \frac{\omega_2{}^2}{\omega_1{}^2} = \frac{4.6 \times 10^{17}}{3.05 \times 10^{17}} = 1.46{:}1$

A capacitance ratio of 1.6 was used to assure covering the FM band with component parameter variations.

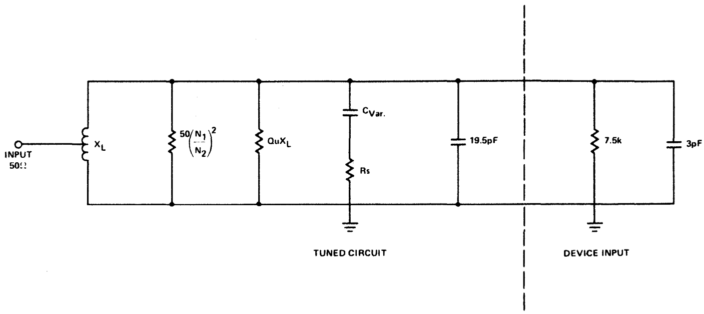


FIGURE 4
INPUT TUNED CIRCUIT

NOTE: ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS.

The equivalent circuit can be further simplified as shown in Figure 5.

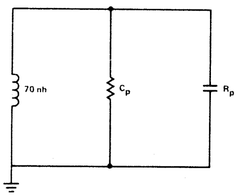


FIGURE 5
SIMPLIFIED INPUT CIRCUIT

NOTE: ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS.

C_p is made up of the D-MOS input capacitance, a fixed parallel capacitor, and the varactors. The maximum C_p required is

$$C_{p1} = \frac{1}{\omega_1{}^2 L} = 47.5\text{pF}.$$

Of this total the capacitance of the varactor is approximately 28pF. This corresponds to a tuning voltage of approximately 2.5V for the varactors used (MV104). Dual varactors in a back-to-back configuration were used so nonlinearities caused by the diodes would cancel.

The minimum C_p required (at 108 MHz) is

$$C_{p_2} = \frac{1}{\omega_2{}^2 L} = 31\text{pF}.$$

The capacitance of the varactor should now be approximately 11.5pF, corresponding to a tuning voltage of 20 volts. The choice of this tuning voltage range is quite arbitrary and just depends on the type of varactors used. For the automobile radio market, a lower voltage varactor could be used. It is possible to tune 88 → 108 MHz with 2 to 10 volts using commercially available varactors.

R_p in Figure 5 is made up of the equivalent parallel resistance of the device input and the parallel resistance of the varactors and the inductor. In this case R_p is approximately equal to 7.5k (device), 5.7k (inductor), and 50k (varactor). This 3.05k parallel resistance is matched to the antenna impedance (in this case it was matched to a 50Ω generator) by tapping the inductor. The required turns ratio is $(3050/50)^{1/2}$ or approximately 7:1.

The bandwidth of the input circuit can be found knowing the total parallel resistance and parallel capacitance

$$B\omega_{-3dB} = \frac{1}{2\pi RC} = \frac{1}{2\pi \times 2k \times 40pF}$$

(at 100 MHz) 3 MHz

This bandwidth is narrow enough to provide good rejection to signals outside the FM band but wide enough to avoid tracking problems.

OUTPUT CIRCUIT

The design of the output circuit is very similar to that of the input. The only difference is a different value of fixed capacitance to take into account the RF amplifier output capacitance and that of the mixer input.

GAIN AND STABILITY

Dual gate D-MOS transistors are exceptionally stable RF devices because of the low feedback capacitance (.02pF typical). This makes it possible to achieve high gain without the need for neutralization. Low feedback also makes AGC possible over a wide dynamic range.

In the FM band, the SD6000 is not unconditionally stable. k, the stability factor, (inverse of Linvill stability factor) is approximately .36. To assure stability, without neutralization, the gain should be limited to about 20dB. In this design the approach chosen was to mismatch the RF amplifier output and the mixer input. This is done by connecting the RF output tank circuit directly to the mixer input (gate 1). This mismatch limits the RF amplifier gain to 18dB and gives a stability factor of 1.27, assuring stable operating conditions.

AGC

Another advantage of the SD6000 is that the input impedance remains essentially constant with AGC level. This means that bandwidth and center frequency do not shift. Figure 6 shows the bandpass characteristics of the completed tuner as different AGC voltages are applied to gate 2 of the RF amplifier.

Figure 7 shows the bandpass characteristics as the RF input frequency is changed.

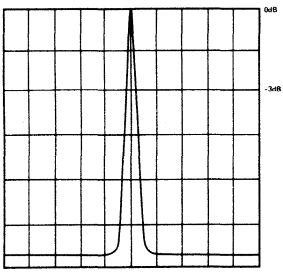
MIXER

The second dual gate D-MOS transistor in the package is used for a mixer. This device was designed especially for mixer applications, and has a wide square law region. The L.O. is injected in gate two and the input signal in gate one. Injecting the L.O. at gate 2 provides the highest isolation of the L.O. signal to the RF input. This isolation is very important because of restrictions on the amount of L.O. power that may be radiated from the tuner antenna.

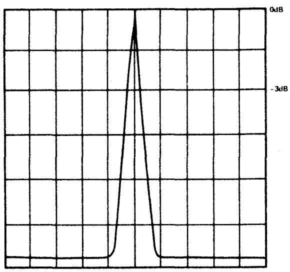
The mixer was designed to operate in the most linear portions of the forward transconductance curves. Figures 8 and 9 show the transconductance curves for the SD6000 are linear in a fairly wide operating region, making this device ideal for mixing. Non-linearities in these curves indicate that third order (and higher) terms would be present if the device was biased in these regions. These higher order terms contribute only to undesired responses. As the transconductance curves become linear, the higher order terms disappear and conversion gain increases.

Figure 8 shows that the gate 1 transconductance curve is almost a straight line for gate 2 bias voltages between 2.0 and 6.0 volts. Figure 9 shows the gate 2 transconductance is linear for gate 1 bias from 2.5 to 3.5 volts.

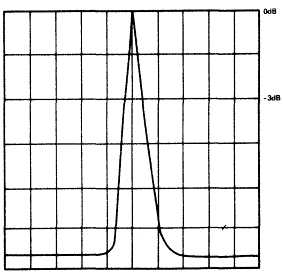
FIGURE 6
AGC/BANDWIDTH CHARACTERISTICS



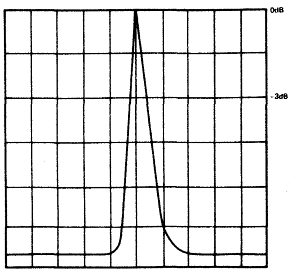
6A. fo = 100 MHz
fif = 10.7 MHz (1 MHz/cm)
V_{AGC} = 10V
Gain Reduction = 0dB



6B. fo = 100 MHz
fif = 10.7 MHz (1 MHz/cm)
V_{AGC} = 3.9v
Gain Reduction = 10dB

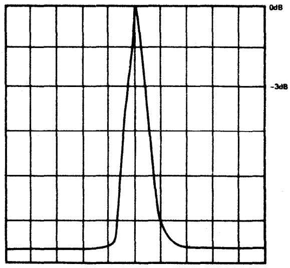


6C. fo = 100 MHz
fif = 10.7 MHz (1 MHz/cm)
V_{AGC} = 2.6v
Gain Reduction = 20dB

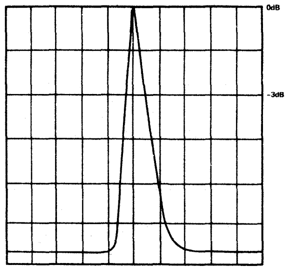


6D. fo = 100 MHz
fif = 10.7 MHz (1 MHz/cm)
V_{AGC} = 1.8v
Gain Reduction = 30dB

FIGURE 6
AGC/BANDWIDTH CHARACTERISTICS
(Continued)

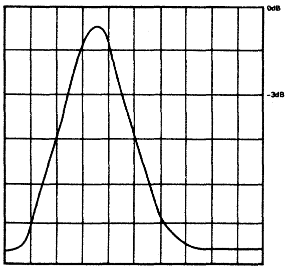


6E. fo = 100 MHz
fif = 10.7 MHz (1 MHz/cm)
V_{AGC} = 1.3v
Gain Reduction = 40dB

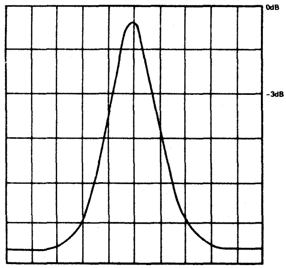


6F. fo = 100 MHz
fif = 10.7 MHz (1 MHz/cm)
V_{AGC} = 0.9v
Gain Reduction = 50dB

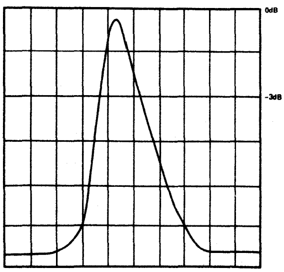
FIGURE 7
BANDWIDTH CHARACTERISTICS



7A. fo = 88 MHz
x = 300 kHz/cm
V_{AGC} = 10v
V_{Tuning} = 3.0v



7B. fo = 100 MHz
x = 300 kHz/cm
V_{AGC} = 10v
V_{Tuning} = 9.8v



7C. fo = 108 MHz
x = 300 kHz/cm
V_{AGC} = 10v
V_{Tuning} = 21.9v

FIGURE 8
SD6000 MIXER

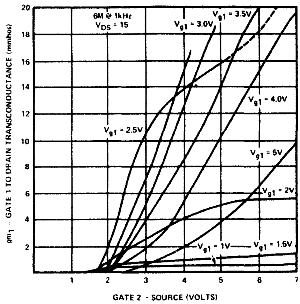
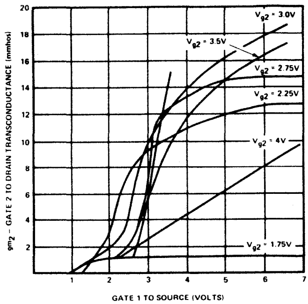


FIGURE 9
SD6000 MIXER



By definition the transconductance, gm is the partial derivative of drain current, i_d, with respect to the input voltage e_s. The total drain current of the mixer can be expressed by

$$i_d = gm_1 V_{g1} + gm_2 V_{g2}$$

where gm_1 = transconductance gate 1 to drain.
gm_2 = transconductance gate 2 to drain.

From Figure 8 the gate 1 transconductance, gm_1 can be expressed as:

$$gm_1 = -17.6 + 8.2 (V_{g2} + v_{g2}) \text{ (mmhos)}$$
for V_{g2} = 2v to 6v

From Figure 9 we get the following expression for gm_2

$$gm_2 = -23.7 + 10.2 (V_{g1} + v_{g1}) \text{ (mmhos)}$$
for V_{g1} = 2.5v to 3.5v

If the DC bias points are chosen, for example V_{g1} = 3.5 and V_{g2} = 3.5, the following expressions are derived from gm_1 and gm_2 using the previous equations

$$gm_1 = 11.1 + 8.2 v_{g2} \text{ (mmhos)}$$
$$gm_2 = 8.9 + 10.2 v_{g1} \text{ (mmhos)}$$

Substituting these equations into the expression for the total drain current, i_d, we get

$$i_d = 11.1 v_{g1} + 8.9 v_{g2} + 18.4 v_{g1} v_{g2}$$

The last term in this equation is the one that will contain the IF frequency we desire. If we let v_{g1} and v_{g2} equal a sinusoidal voltage, v_{g1} is the input signal voltage and v_{g2} is the local oscillator, we obtain

$$v_{g1} = E_s \sin \omega_s t$$
$$v_{g2} = E_{LO} \sin \omega_{LO} t$$

Substituting v_{g1} and v_{g2} into the equation for i_d gives

$$i_d = 18.4 E_S E_{LO}$$
$$[1/2 \cos (\omega_{LO} + \omega_s) t + 1/2 \cos (\omega_{LO} - \omega_s) t]$$

The $(\omega_{LO} - \omega_s)$ term is the 10.7 MHz IF we want. Dividing both sides of the equation by E_s we obtain

$$\frac{i_d}{E_s} = gm_c = 9.2 E_{LO} \text{ (peak)}$$
$$= 13 E_{LO} \text{ (RMS) mmhos}$$

This exercise shows that relatively high conversion gains can be achieved using the SD6000. It can be seen that the conversion transconductance will also be a function of the local oscillator level.

In the tuner that was constructed, a local oscillator level of 800mV RMS was chosen. This gives a conversion transconductance of 10.4 mmhos. The conversion power gain can be calculated by

$$Pg = \frac{|gm_c|^2 R_{in} R_{out}}{4}$$

$$Pg = \frac{[10.4X 10^{-3}]^2 [2k] [2k]}{}$$

$$\approx 109 = 20.4\text{dB}$$

This calculated result compares closely with that measured in the actual tuner.

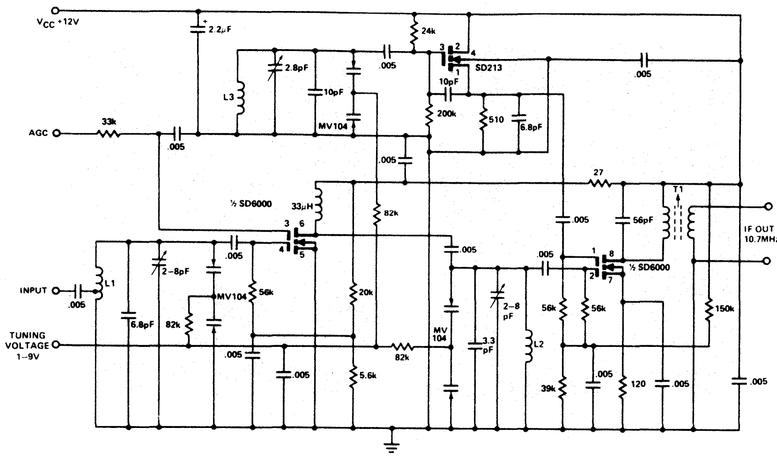
TUNER PERFORMANCE

A schematic of the tuner built with the SD6000 is shown in Figure 10. Figure 11 shows the printed circuit board layout.

At the present time complete measurements have not been made to verify the tuner performance. A summary of the data that has been measured is given below:

V_{Supply} = +12V
V_{AGC} = 0→+10V Sensitivity (30dB quieting) $<1.5\mu V$

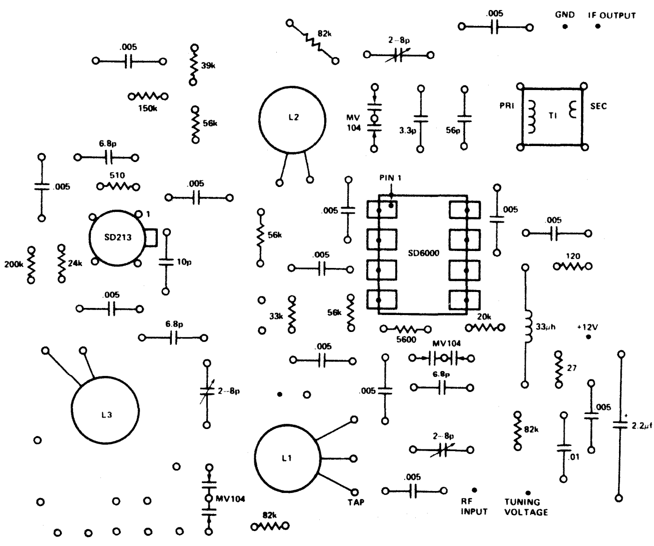
Frequency (MHz)	Tuning Voltage (VDC)	Gain (dB)	AGC Range (dB)
88	1.2	30	>50
92	2.2	32	>50
96	3.0	34	>50
100	4.1	33	>50
104	5.9	32	>50
108	8.7	31	>50



NOTE: ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS.

L1 – 5 TURNS #22 ON T37–12 CORE TAP 1 TURN FROM GND
L2 – 5 TURNS #22 ON T37–12 CORE
L3 – 4 TURNS #22 ON T37–12 CORE
T1 – 533-3652-003 CAMBION
PRI. – 30 TURNS #26
SEC. – 2 TURNS #26

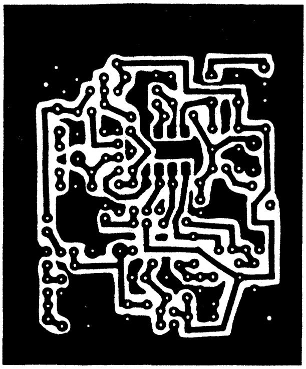
FIGURE 10
DMOS VARACTOR TUNER



NOTE: ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS.

FIGURE 11A
COMPONENT LAYOUT

BOTTOM VIEW



TOP VIEW

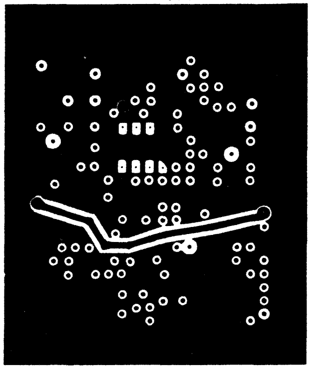


FIGURE 11B
PC BOARD LAYOUT

LOCAL OSCILLATOR

The design of the local oscillator used in this tuner is explained in Appendix A. The SD213 was used because of its linearity and therefore low harmonic generation.

CONCLUSIONS

Preliminary performance data indicates that in an FM tuner dual D-MOS will give the high performance required in modern FM radios. The sensitivity and spurious response should exceed that of the best bipolars.

APPENDIX A

ANALYSIS OF COMMON DRAIN D-MOS OSCILLATOR

This report describes a simplified analysis for a Colpitts oscillator using a Signetics D-MOS transistor in the common drain configuration. The D-MOS device parameters are more stable than those of a bipolar device under temperature and supply voltage variations giving an improvement in frequency stability. The D-MOS devices are also inherently linear and therefore reduce the generation of harmonics of the fundamental oscillator frequency.

Figure 1 shows the equivalent circuit for the dual gate D-MOS transistor.

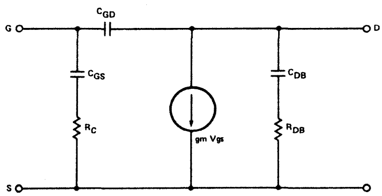


FIGURE 1
D-MOS EQUIVALENT CIRCUIT

NOTE: ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS.

In this analysis the equivalent circuit shown in Figure 2 will be used. This simplification is justified in this case because the device capacitances are small compared to external capacitances and the equivalent parallel real impedances are very high.

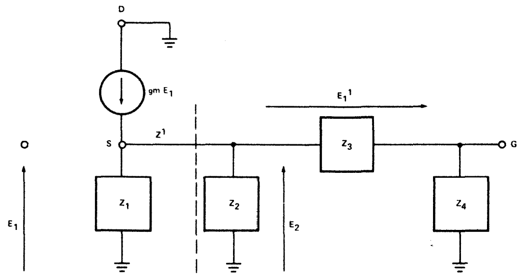


FIGURE 2
COMMON DRAIN D-MOS OSCILLATOR EQUIVALENT CIRCUIT

NOTE: ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS.

The following analysis will show a solution for Z_1, Z_2, Z_3, and Z_4 which satisfies the Barkhausen criterion for oscillation.

$$Z' = \frac{Z_2 (Z_3 + Z_4)}{Z_2 + Z_3 + Z_4}$$

$$E_2 = \frac{gm\, Z_1\, Z'\, E_1}{Z_1 + Z'}$$

$$E_1' = -\frac{E_2\, Z_3}{Z_3 + Z_4}$$

substituting E_2

$$E_1' = -\frac{gm\, Z_1\, Z'\, E_1\, Z_3}{(Z_1 + Z')(Z_3 + Z_4)}$$

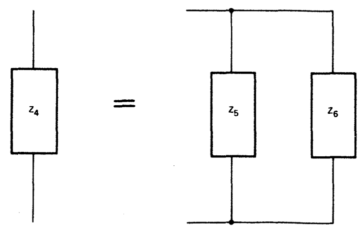
dividing both sides by E_1

$$\frac{E_1'}{E_1} = -\frac{gm\, Z_1\, Z_3\, Z'}{(Z_1 + Z')(Z_3 + Z_4)}$$

substituting Z'

$$\frac{E_1'}{E_1} = \frac{-\, gm\, Z_1\, Z_2\, Z_3}{Z_1 (Z_2 + Z_3 + Z_4) + Z_2 (Z_3 + Z_4)}$$

let



then $Z_4 = \dfrac{Z_5 Z_6}{Z_5 + Z_6}$

substitute Z_4 into $\dfrac{E_1'}{E_1}$

$$\frac{E_1'}{E_1} = \frac{-gm\, Z_1\, Z_2\, Z_3\, (Z_5 + Z_6)}{Z_1\, [Z_2\, (Z_5 + Z_6) + Z_3\, (Z_5 + Z_6) + Z_5\, Z_6] + Z_2\, [Z_3\, (Z_5 + Z_6) + Z_5\, Z_6]}$$

for the Colpitts oscillator configuration choose

$Z_1 = R$
$Z_2 = -jX_2$
$Z_3 = -jX_3$
$Z_5 = jX_5$
$Z_6 = -jX_6$

therefore

$$\frac{E_1'}{E_1} = \frac{-gm\, R\, X_2\, X_3\, (X_5 - X_6)}{X_2\, [(X_3\, (X_5 - X_6) + X_5\, X_6] + jR\, [X_2\, (X_5 - X_6) + X_3\, (X_5 - X_6) + X_5\, X_6]}$$

to satisfy the Barkhausen criterion

$$\frac{E_1'}{E_1} = 1\angle 0^\circ$$

therefore for the imaginary part of $\dfrac{E_1'}{E_1}$ to be equal to zero

$$X_2\, X_5 + X_3\, X_5 + X_5\, X_6 = X_2\, X_6 + X_3\, X_6$$

or $X_5 = \dfrac{X_6\, (X_2 + X_3)}{X_2 + X_3 + X_6}$

This means that the oscillator frequency will be determined by the series combination of X_2 and X_3 in parallel with X_6 and resonating with X_5.

For oscillation to occur the magnitude of $\dfrac{E_1'}{E_1}$ must be equal to or greater than unity. Therefore

$$\left| \frac{-gmR\, X_2\, X_3\, (X_5 - X_6)}{X_2\, [X_3\, (X_5 - X_6) + X_5\, X_6]} \right| \geqslant 1$$

which simplifies to

$gmR \geqslant \dfrac{X_2}{X_3}$

or $gmR \geqslant \dfrac{C_3}{C_2}$ using the expression derived for X_5.

An oscillator for use in a varactor tuned FM receiver was designed using this configuration. A schematic of the circuit is shown in Figure 3.

NOTE: ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS.

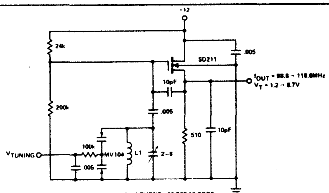


FIGURE 3
D-MOS FM TUNER LOCAL OSCILLATOR

SALES OFFICES

AUSTRIA
Österreichische Philips,
Bauelemente Industrie G.m.b.H.,
Zieglergasse 6,
Tel. 93 26 11, A-1072 WIEN.

BELGIUM
M.B.L.E.,
80, rue des Deux Gares,
Tel. 523 00 00,
B-1070 BRUXELLES.

DENMARK
Miniwatt A/S,
Emdrupvej 115A,
Tel. (01) 69 16 22,
DK-2400 KØBENHAVN NV.

FINLAND
Oy Philips Ab,
Elcoma Division,
Kaivokatu 8,
Tel. 1 72 71,
SF-00100 HELSINKI 10.

FRANCE
R.T.C.,
La Radiotechnique-Compelec,
130 Avenue Ledru Rollin,
Tel. 355-44-99,
F-75540 PARIS 11.

GERMANY
Valvo,
U.B. Bauelemente der Philips
G.m.b.H.,
Valvo Haus,
Burchardstrasse 19,
Tel. (040) 3296-1,
D-2 HAMBURG 1.

GREECE
Philips S. A. Hellénique,
Elcoma Division,
52 Av. Syngrou,
Tel. 915 311, ATHENS.

IRELAND
Philips Electrical (Ireland) Ltd.,
Newstead,
Clonskeagh,
Tel. 69 33 55, DUBLIN 14.

ITALY
Philips S.p.A.,
Sezione Elcoma,
Piazza IV Novembre 3,
Tel. 2-6994, I-20124 MILANO.

NETHERLANDS
Philips Nederland B.V.,
Afd. Elonco,
Boschdijk 525,
Tel. (040) 79 33 33,
NL-4510 EINDHOVEN.

NORWAY
Electronica A.S.,
Vitaminveien 11,
Tel. (02) 15 05 90,
P.O. Box 29, Grefsen, OSLO 4.

PORTUGAL
Philips Portuguesa S.A.R.L.,
Av. Eng. Duharte Pacheco 6,
Tel. 68 31 21, LISBOA 1.

SPAIN
COPRESA S.A.,
Balmes 22,
Tel. 329 63 12, BARCELONA 7.

SWEDEN
ELCOMA A.B.,
Lidingövägen 50,
Tel. 08/67 97 80,
S-10 250 STOCKHOLM 27.

SWITZERLAND
Philips A.G.,
Edenstrasse 20,
Tel. 01/44 22 11,
CH-8027 ZUERICH.

TURKEY
Türk Philips Ticaret A.S.,
EMET Department,
Gümüssuyu Cad. 78-80,
Tel. 45.32.50, Beyoglü,
ISTANBUL.

UNITED KINGDOM
Mullard Ltd.,
Mullard House,
Torrington Place,
Tel. 01-580 6633,
LONDON WC1E 7HD.

signetics

the IC professionals